IEI Integration Corp.

MODEL:

PCIE-RPL-Q670

Full-size PICMG 1.3 CPU Card supports LGA1700 Intel® 12th/13th/14th Gen. Core™ i9/i7/i5/i3/Pentium®/Celeron® CPU with Q670E, DDR5, HDMI, DP, Dual Intel® 2.5GbE, USB 3.2, SATA 6Gb/s, M.2, HD Audio and RoHS

User Manual

Rev. 1.00 – Sep 9, 2024

RoHS Lead Free

Revision

Date	Version	Changes
Sep 9, 2024	1.00	Initial release

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Manual Conventions

WARNING

Warnings appear where overlooked details may cause damage to the equipment or result in personal injury. Warnings should be taken seriously.

CAUTION

Cautionary messages should be heeded to help reduce the chance of losing data or damaging the product.

NOTE

These messages inform the reader of essential but non-critical information. These messages should be read carefully as any directions or instructions contained therein can help avoid making mistakes.

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Introduction

1.1 Introduction

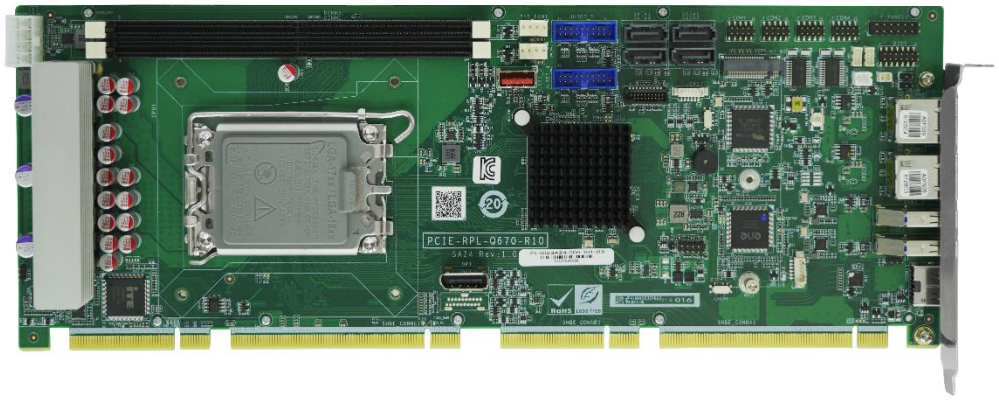


Figure 1-1: PCIE-RPL-Q670

The PCIE-RPL-Q670 is a full-size PICMG 1.3 CPU card. It is powered by 12th/13th/14th Generation Intel® Core™ i9/i7/i5/i3, Pentium® or Celeron® processor and two 288-pin 5200MHz dual-channel DDR5 DIMMs (up to 96GB). The integrated Intel® Q670E chipset supports four SATA 6Gb/s drives with RAID 0/1/5/10 function.

The PCIE-RPL-Q670 provides two 2.5GbE interfaces through the Intel® I226-V/ I226-LM controllers. Expansion and I/O include one M.2 slots, three USB 3.2 Gen 2 ports by USB Type-A port and four USB 3.2 Gen 1, four USB 2.0 to backplane, two RS-232 and two RS-232/422/485 via internal pin headers.

1.2 Features

The PCIE-RPL-Q670 motherboard features are listed below:

- Full-size PICMG 1.3 CPU card
- LGA1700 12th/13th/14th Generation Intel® Core™ i9/i7/i5/i3, Pentium® or Celeron® processor supported
- Intel® Q670E chipset
- Two 288-pin 5200 MHz dual-channel unbuffered DDR5 SDRAM DIMMs supported up to 96GB
- Two Intel® I226V/I226-LM 2.5GbE controller
- One M.2 2242/2280 M-key slot for storage
- Four SATA 6Gb/s connectors support RAID 0, 1, 5, 10 function
- Three USB 3.2 Gen2, four USB 3.2 Gen 1 and four USB 2.0 to backplane
- Two RS-232/422/485 serial ports via internal pin headers
- Two RS- RS-232 serial ports via internal pin headers
- TPM 2.0 security function supported by PTT (Platform Trust Technology)，based on BIOS setting
- RoHS compliant

1.3 Connectors

The connectors on the PCIE-RPL-Q670 are shown in the figure below.

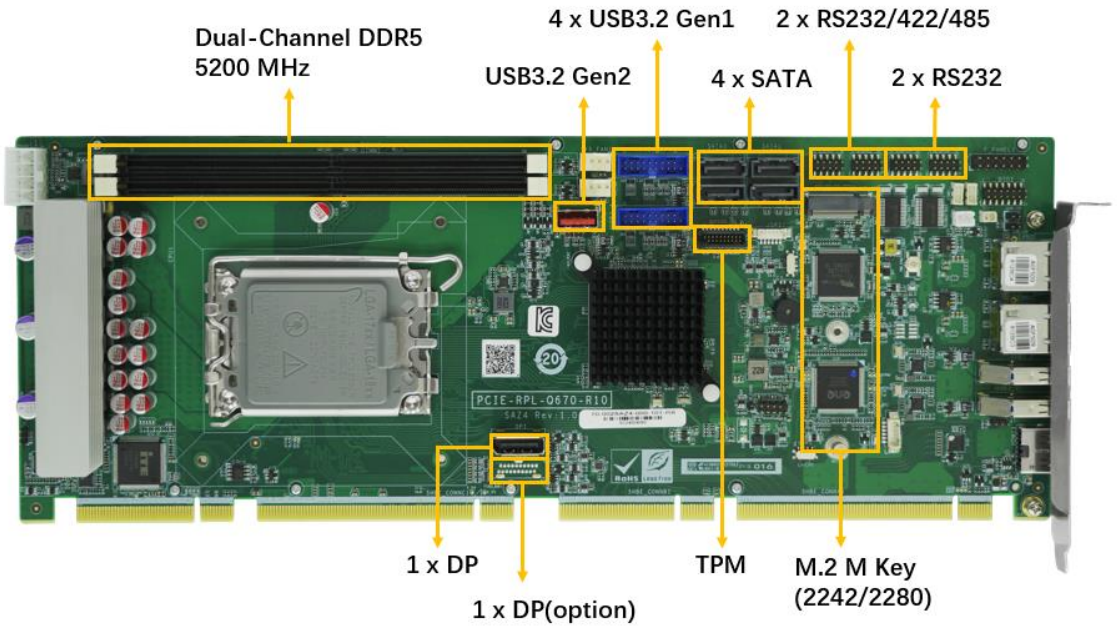


Figure 1-2: Connectors

1.4 Dimensions

The main dimensions of the PCIE-RPL-Q670 are shown in the diagram below.

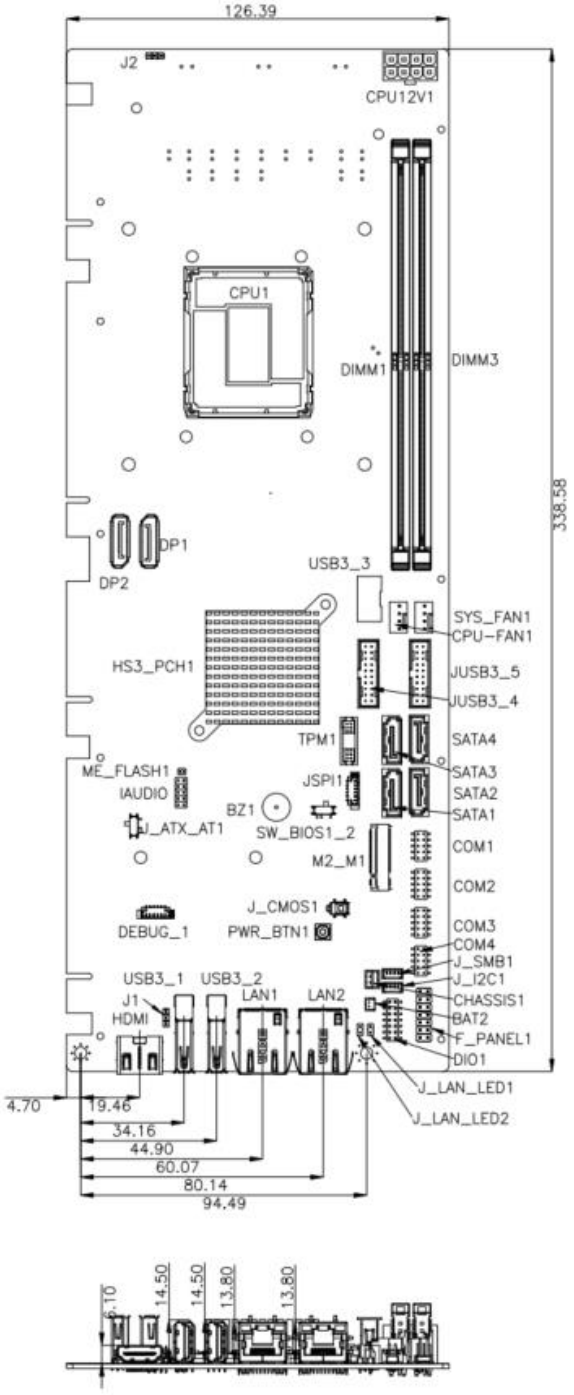


Figure 1-3: PCIE-RPL-Q670 Dimensions (mm)

1.5 Data Flow

Figure 1-4 shows the data flow between the system chipset, the CPU and other components installed on the motherboard.

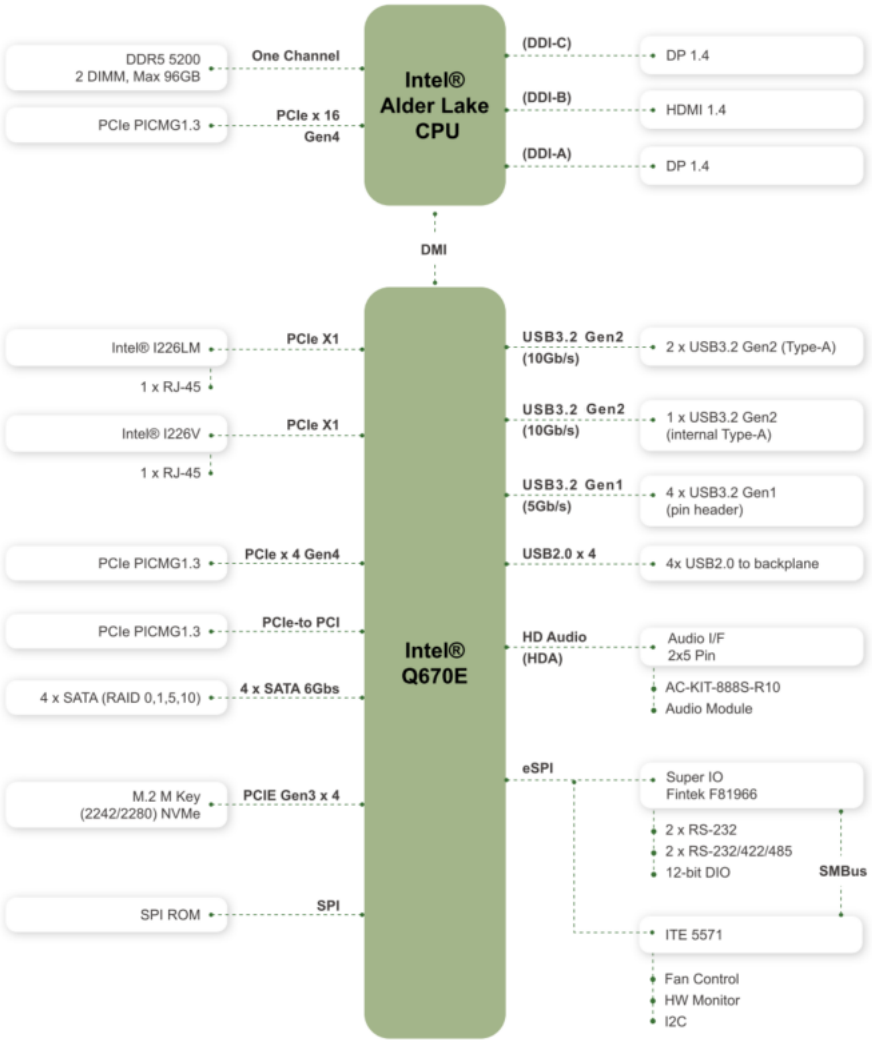


Figure 1-4: Data Flow Diagram

1.6 Technical Specifications

The PCIE-RPL-Q670 technical specifications are listed below.

Specification/Model	PCIE-RPL-Q670
Form Factor	Full-size PICMG 1.3 CPU Card
CPU Supported	LGA1700 socket supports 12th/13th/14th generation Alder Lake-S Intel® Core® i9/i7/i5/i3/Pentium®/Celeron® Processor（up to 65W)
PCH	Intel® Q670E
Memory	Two 288-pin 5200 MHz Dual-Channel DDR5 SDRAM Unbuffered DIMMs supported up to 96GB
Graphics Engine	New Intel® Xe Graphics architecture with SRIOV, Genlock
Display Output	Triple independent display 1 x HDMI 1.4 (up to 4096 x 2304 @30Hz) 1 x interface DP 1.4 (up to 4096 x 2304 @60Hz) 180°（DP++） **1 x interface DP1.4 (up to 4096 x 2304 @60Hz) 180°（DP++）(option）
Ethernet Controllers	LAN1: Intel® I226-LM 2.5GbE controller LAN2: Intel® I226-V 2.5GbE controller
Audio	1 x iAUDIO, support IEI AC-KIT-888S Audio Module (2 x 5 pin)
BIOS	AMI UEFI BIOS
Expansions	1 x M.2 M Key (2242/2280, PCIe Gen3 x4) NVMe support 1 x PCIe Gen3 x16 & 4 x PCIe Gen3 x1 signal via golden finger 4 x PCI signal via golden finger
Watchdog Timer	Software programmable supports 1~255 sec. system reset
I/O Interface Connectors	
Chassis Intrusion	1 x Chassis intrusion (1x2 pin)

Digital I/O	1 x 12-bit digital I/O (2x7 pin)
Ethernet	Two RJ-45 GbE ports
Fan	1 x CPU fan connector (1x4 pin) 1 x System fan connector (1x4 pin)
Front Panel	1 x Front panel connector (2x7 pin) Power LED, HDD LED, power button, reset button
I²C	One 4-pin wafer connector
LAN LED	2 x LAN LED (1x2 pin)
Serial ATA	4 x SATA 6Gb/s connectors (support RAID 0, 1, 5, 10)
Serial Ports	2 x RS-232/422/485 (2x5 pin, P=2.54) (RS485 support AFC) 2 x RS-232 (2x5 pin, P=2.54)
SMBus	One 4-pin wafer connector
TPM	Support TPM 2.0(TPM-IN03 module) & Intel PTT
USB Ports	1 x USB 3.2 Gen2 (Type A 180°) 4 x USB 3.2 Gen1 (2 X 10PIN P=2.00 pin wafer) (5Gb/s) 4x USB 2.0 to backplane 2 x USB 3.2 Gen2 (Type-A) (10Gb/s)
Environmental and Power Specifications	
Power Supply	ATX/AT power supply Support AT/ATX mode ErP/EuP Compliant
Power Consumption	3.3V@2.39A, 5V@9.68A, 12V@6.56A, 5VSB@0.35A (Intel® Core™ i9-12900 CPU with 16 GB 5600 MHz DDR5 memory, EuP mode disabled)
Operating Temperature	-10ºC ~ 60ºC
Storage Temperature	-30ºC ~ 70ºC
Operating Humidity	5% ~ 95% (non-condensing)
Physical Specifications	

Dimensions	338 mm x 126 mm
Weight (GW/NW)	GW:1000g / NW:500g
Certification	CE/FCC compliant

**The DP interface is not plugged in. If needed, MOQ is 100.

Table 1-1: PCIE-RPL-Q670 Specifications

Chapter

2

Packing List

2.1 Anti-static Precautions

WARNING!

Static electricity can destroy certain electronics. Make sure to follow the ESD precautions to prevent damage to the product, and injury to the user.

Make sure to adhere to the following guidelines:

- ***Wear an anti-static wristband***: Wearing an anti-static wristband can prevent electrostatic discharge.
- ***Self-grounding***: Touch a grounded conductor every few minutes to discharge any excess static buildup.
- ***Use an anti-static pad***: When configuring any circuit board, place it on an anti-static mat.
- ***Only handle the edges of the PCB***: Don't touch the surface of the motherboard. Hold the motherboard by the edges when handling.

2.2 Unpacking Precautions

When the PCIE-RPL-Q670 is unpacked, please do the following:

- Follow the anti-static guidelines above.
- Make sure the packing box is facing upwards when opening.
- Make sure all the packing list items are present.

2.3 Packing List

NOTE:

If any of the components listed in the checklist below are missing, do not proceed with the installation. Contact the IEI reseller or vendor the PCIE-RPL-Q670 was purchased from or contact an IEI sales representative directly by sending an email to sales@ieiworld.com.

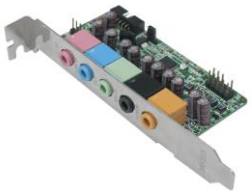
The PCIE-RPL-Q670 is shipped with the following components:

Quantity	Item and Part Number	Image
1	PCIE-RPL-Q670 CPU card	
1	SATA cable	
1	Quick installation guide	

Table 2-1: Packing List

2.4 Optional Items

The following are optional components which may be separately purchased:

Item and Part Number	Image
USB 3.0 cable 450mm with bracket, P=2.0 (**P/N**: 19800-010500-200-RS)	
SATA power cable, 200mm, P=2.0 (**P/N**: 32102-000100-200-RS)	
RS-232/422/485 cable, 300mm, P=2.00, with bracket (**P/N**: 19800-000200-100-RS)	
TPM2.0 module, software mangement tool (**P/N**: TPM-IN03-R10)	
Realtek ALC888S 7.1 Channel HD Audio peripheral board (**P/N**: AC-KIT-888S-R10)	
High-performance LGA1700 cooler, 65W (72 x 70 x 25.5 mm) (**P/N**: 19100-000323-00-RS)	

Item and Part Number	Image
High-performance 1 U LGA1700 cooler, 65W (95 x 90 x 27.45 mm) (**P/N**: 19100-000319-00-RS)	

Table 2-2: Optional Items

Chapter

3

Connectors

3.1 Peripheral Interface Connectors

This chapter details all the peripheral interface connectors.

3.1.1 PCIE-RPL-Q670 Layout

The figure below shows all the peripheral interface connectors.

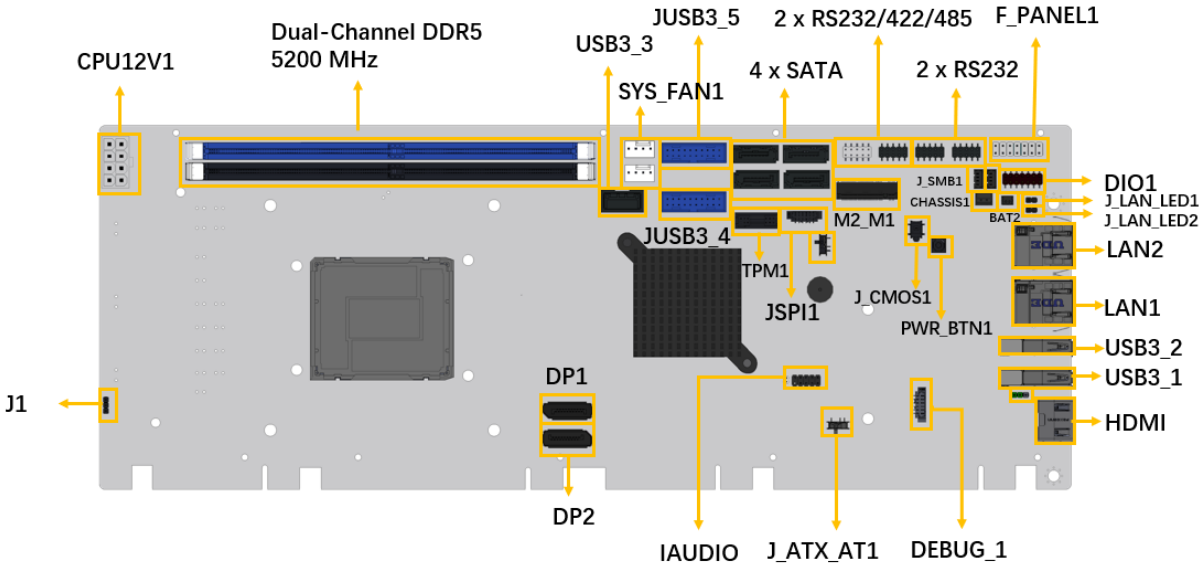


Figure 3-1: Peripheral Interface Connectors

3.1.2 Peripheral Interface Connectors

The table below lists all the connectors on the board.

Connector	Type	Label
ATX CPU 12V power connector	8-pin Molex power connector	CPU12V1
Battery connector	2-pin wafer	BAT2
Chassis intrusion connector	2-pin header	CHASSIS1
AT/ATX power mode setting	3-pin switch	J_ATX_AT1
Digital I/O connector	14-pin header	DIO1
EC debug connector	6-pin wafer	DEBUG_1
Clear CMOS jumper	Push button	J_CMOS1
Flash descriptor security override jumper	2-pin header	ME_FLASH1
Fan connectors (CPU)	4-pin wafer	CPU_FAN1
Fan connectors (system)	4-pin wafer	SYS_FAN1
BIOS selection switch	3-pin switch	SW_BIOS1_1
Audio connector	10-pin header	IAUDIO
Front panel connector	14-pin header	F_PANEL1
I²C connector	4-pin wafer	J_I2C1
SMBus connector	4-pin wafer	J_SMB1
LAN1 link LED connector	2-pin header	JLED_LED1
LAN2 link LED connector	2-pin header	JLED_LED2
Trusted Platform Module connector	20-pin header	TPM1
M.2 M-key slot (on solder side)	M.2 M-key slot	M2_M1
On-board power switch	Push button	PWR_BTN1
DDR5 DIMM slots	288-pin socket	DIMM1 DIMM3
SATA 6Gb/s connectors	7-pin SATA connector	SATA1, SATA2, SATA3, SATA4

Connector	Type	Label
RS-232 serial port connectors	10-pin box header	COM3, COM4
RS-232/422/485 serial port connectors	4-pin wafer	COM1, COM2
Flash SPI ROM connector	6-pin wafer	JSPI1
DP connector	DisplayPort	DP1
Internal USB 3.2 Gen 2 connector (Type-A)	USB 3.2 Gen 1	USB3_3
Internal USB 3.2 Gen 1 connector	20-pin box header	JUSB3_5, JUSB3_4

Table 3-1: Peripheral Interface Connectors

3.1.3 External Interface Panel Connectors

The table below lists the connectors on the external I/O panel.

Connector	Type	Label
External 2.5GbE RJ-45 connectors	Dual RJ-45	LAN1, LAN2
External HDMI connector	HDMI	HDMI
External USB 3.2 Gen 2 connectors	USB 3.2 Gen2 Type-A	USB3_1, USB3_2

Table 3-2: External Peripheral Connectors

3.3 Internal Peripheral Connectors

The section describes all of the connectors on the PCIE-RPL-Q670.

3.3.1 CPU 12V Power Connector

CN Label: **CPU12V1**

CN Type: 8-pin Molex power connector, p=4.2 mm

CN Location: See **Figure 3-2**

CN Pinouts: See **Table 3-3**

This connector provides power to the CPU.

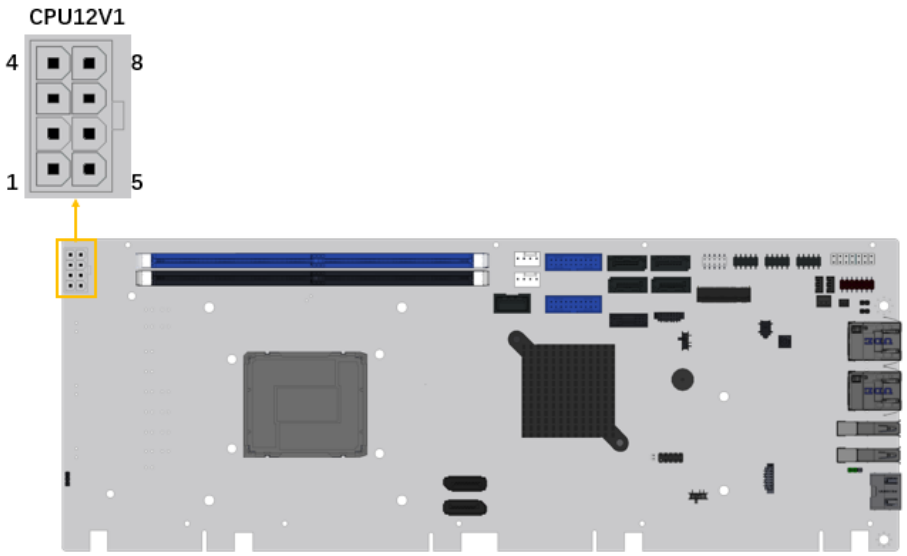


Figure 3-2: ATX CPU 12V Power Connector Location

Pin	Description	Pin	Description
1	GND	5	+12V
2	GND	6	+12V
3	GND	7	+12V
4	GND	8	+12V

Table 3-3: ATX CPU 12V Power Connector Pinouts

3.3.2 Battery Connector

CAUTION:

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

NOTE:

It is recommended to attach the RTC battery onto the system chassis in which the PCIE-RPL-Q670 is installed.

CN Label:	**BAT2**
CN Type:	2-pin wafer, p=1.25 mm
CN Location:	See **Figure 3-3**
CN Pinouts:	See **Table 3-4**

This is connected to the system battery. The battery provides power to the system clock to retain the time when power is turned off.

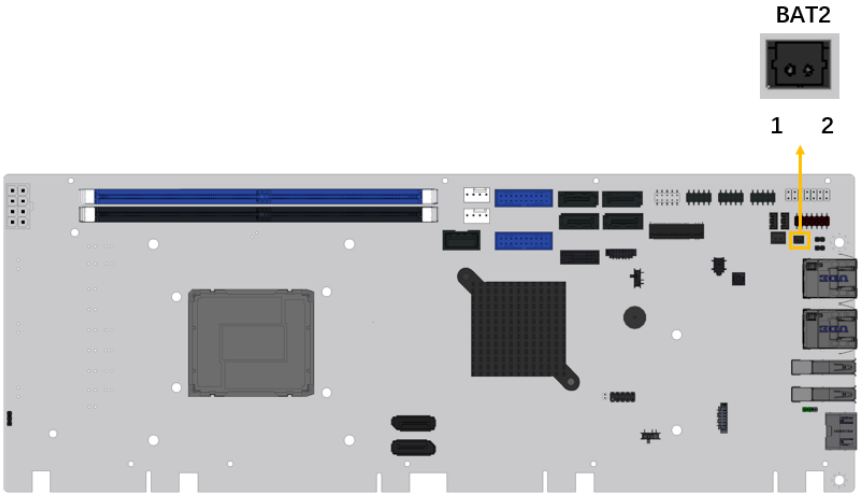


Figure 3-3: Battery Connector Location

Pin	Description	Pin	Description
1	VBATT	2	GND

Table 3-4: Battery Connector Pinouts

3.3.3 AT/ATX Power Mode Setting

CN Label: **J_ATX_AT1**

CN Type: 3-pin switch

CN Location: See **Figure 3-4**Figure 3-10

CN Pinouts: See **Table 3-5**

The AT/ATX power mode selection is made through the AT/ATX power mode switch.

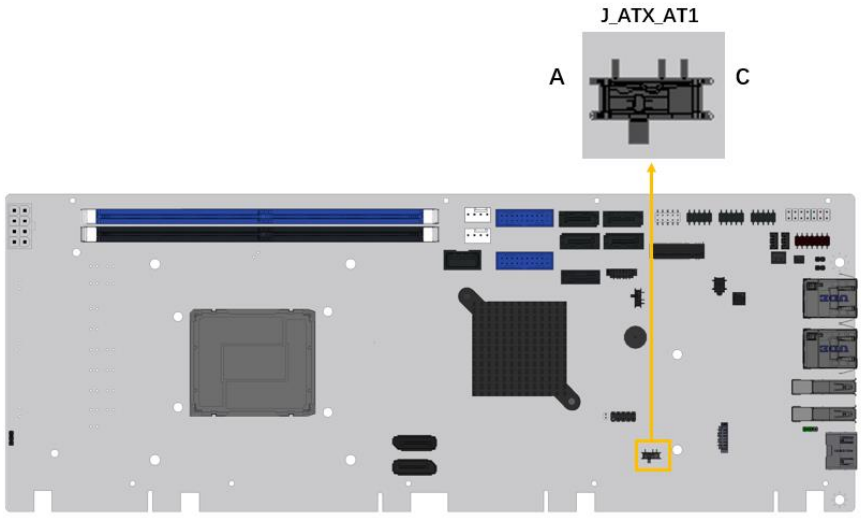


Figure 3-4: AT/ATX Power Mode Switch Locations

Pin	Description	Pin	Description
Short A - B	ATX Power Mode (default)	Short B - C	AT Power Mode

Table 3-5: AT/ATX Power Mode Switch Settings

3.3.4 Clear CMOS Button

CN Label: **J_CMOS1**

CN Type: Button

CN Location: See **Figure 3-5**

CN Pinouts: See **Table 3-6**

The J_CMOS1 is used to Clear CMOS Setup.

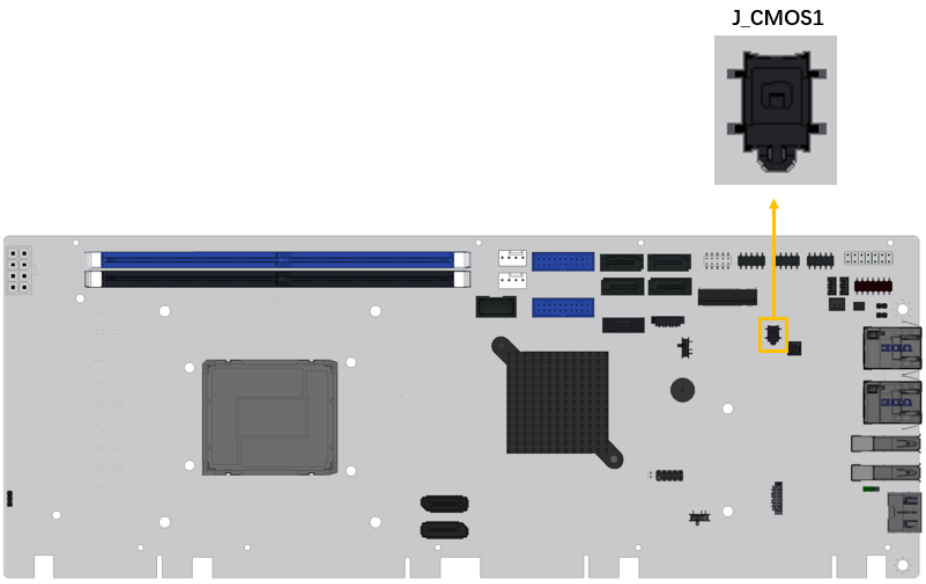


Figure 3-5: Clear CMOS Jumper Location

Pin	Description
NC	Keep CMOS Setup (Normal Operation)
Press button	Clear CMOS Setup

Table 3-6: Clear CMOS Jumper Pinouts

3.3.5 Flash Descriptor Security Override Jumper

CN Label:	**ME_FLASH1**
CN Type:	2-pin header, p=1.27 mm
CN Location:	See **Figure 3-14**
CN Pinouts:	See **Figure 3-15**

The ME_FLASH1 connector is used for Flash Descriptor security override jumper.

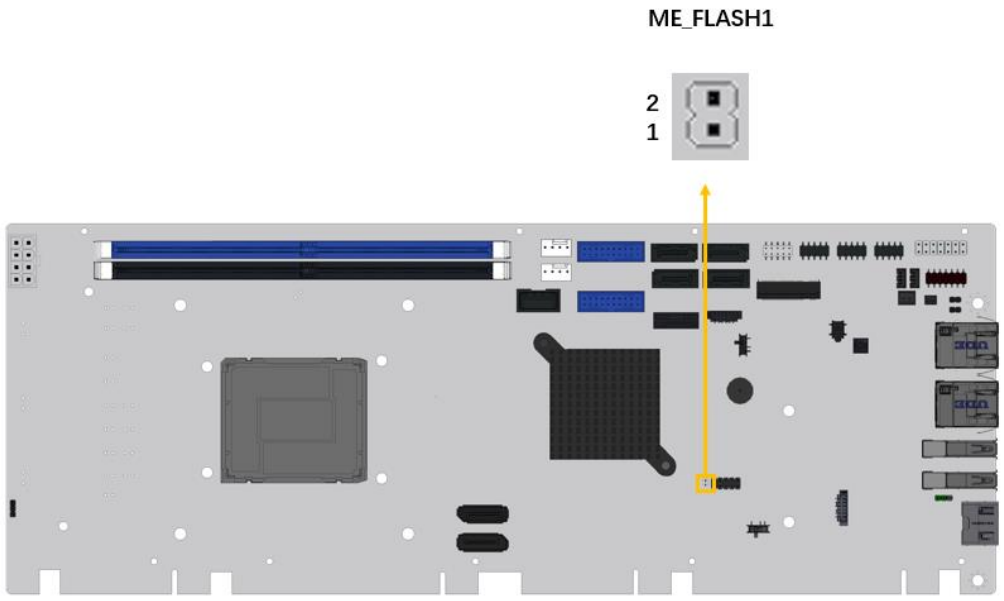


Figure 3-6: Flash Descriptor Security Override Jumper Location

Pin	Description
Open	Disabled (default)
Short	Enabled

Table 3-7: Flash Descriptor Security Override Jumper Pinouts

To update the ME firmware, please follow the steps below.

Step 1: Before turning on the system power, short the Flash Descriptor Security Override jumper.

Step 2: Update the BIOS and ME firmware, and then turn off the system power.

Step 3: Remove the metal clip on the Flash Descriptor Security Override jumper or return to its default setting.

Step 4: Restart the system. The system will reboot 2 ~ 3 times to complete the ME firmware update.

3.3.6 BIOS Selection Switch

CN Label:	**SW_BIOS1_2**
CN Type:	3-pin switch
CN Location:	See **Figure 3-5**
CN Pinouts:	See **Table 3-6**

The BIOS selection is made through the BIOS switch.

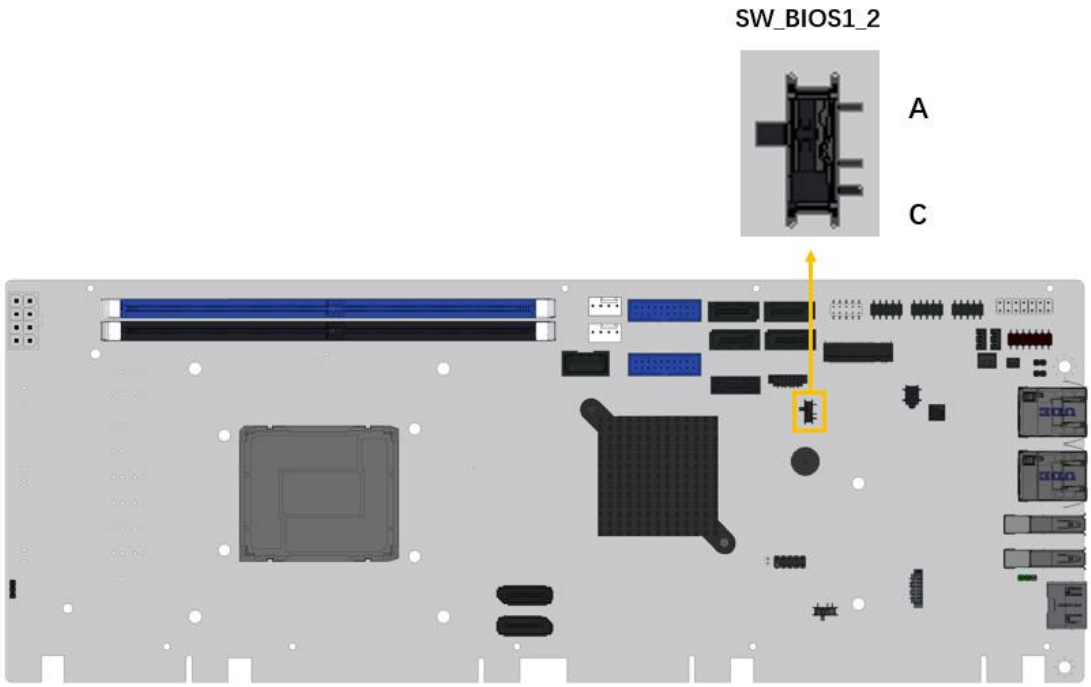


Figure 3-7: BIOS Switch Location

Pin	Description
Short A - B	BIOS1: one PCIe x4 slots (default)
Short B - C	BIOS2: four PCIe x1 slot

Table 3-8: BIOS Switch Pinouts

3.3.7 Chassis Intrusion Connector

CN Label: **CHASSIS1**

CN Type: 2-pin header, p=2.00 mm

CN Location: See **Figure 3-8**

CN Pinouts: See **Table 3-9**

The chassis intrusion connector is for a chassis intrusion detection sensor or switch that detects if a chassis component is removed or replaced.

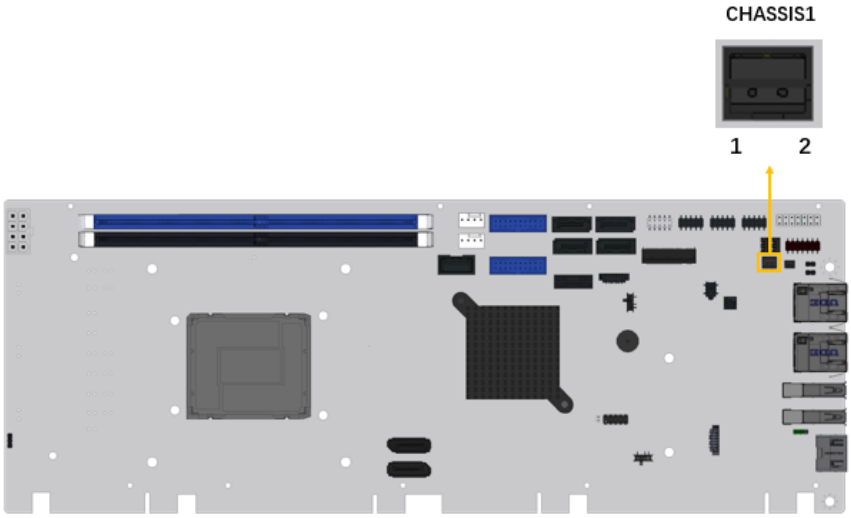


Figure 3-8: Chassis Intrusion Connector Location

Pin	Description
1	CASEOPEN_N
2	GND

Table 3-9: Chassis Intrusion Connector Pinouts

3.3.8 Digital Input /Output Connector

CN Label: **DIO1**

CN Type: 14-pin header, p=2.00 mm

CN Location: See **Figure 3-9**

CN Pinouts: See **Table 3-10**

The digital I/O connector provides programmable input and output for external devices.

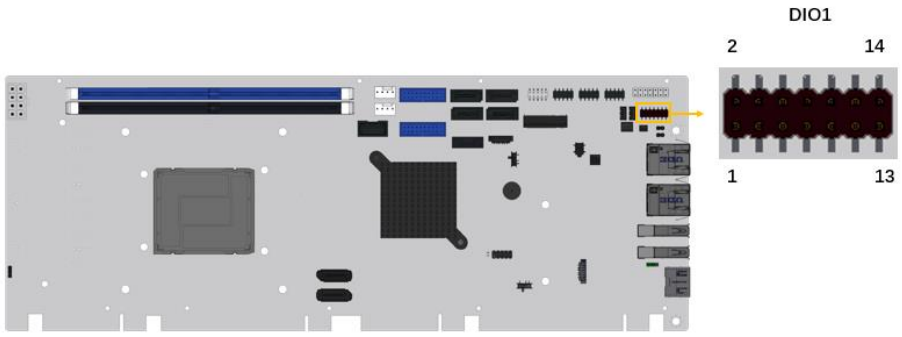


Figure 3-9: Digital I/O Connector Location

Pin	Description	Pin	Description
1	GND	2	+5V
3	DOUT5	4	DOUT4
5	DOUT3	6	DOUT2
7	DOUT1	8	DOUT0
9	DIN5	10	DIN4
11	DIN3	12	DIN2
13	DIN1	14	DIN0

Table 3-10: Digital I/O Connector Pinouts

3.3.9 EC Debug Connector

CN Label: **DEBUG_1**

CN Type: 6-pin wafer, p=1.25 mm

CN Location: See **Figure 3-10**

CN Pinouts: See **Table 3-11**

The EC debug connector is used for EC debug.

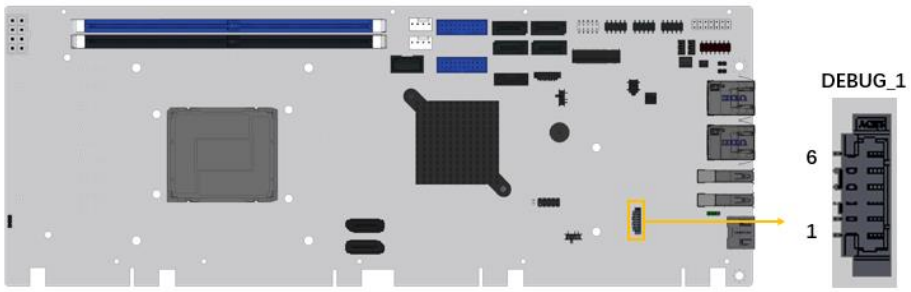


Figure 3-10: EC Debug Connector Location

Pin	Description	Pin	Description
1	NC	2	EDICS
3	EDIDO	4	EDICLK
5	EDIDI	6	GN

Table 3-11: EC Debug Connector Pinouts

3.3.10 Fan Connectors (CPU)

CN Label: **CPU_FAN1**

CN Type: 4-pin wafer, p=2.54 mm

CN Location: See **Figure 3-11**

CN Pinouts: See **Table 3-12**

The fan connector attaches to a CPU cooling fan.

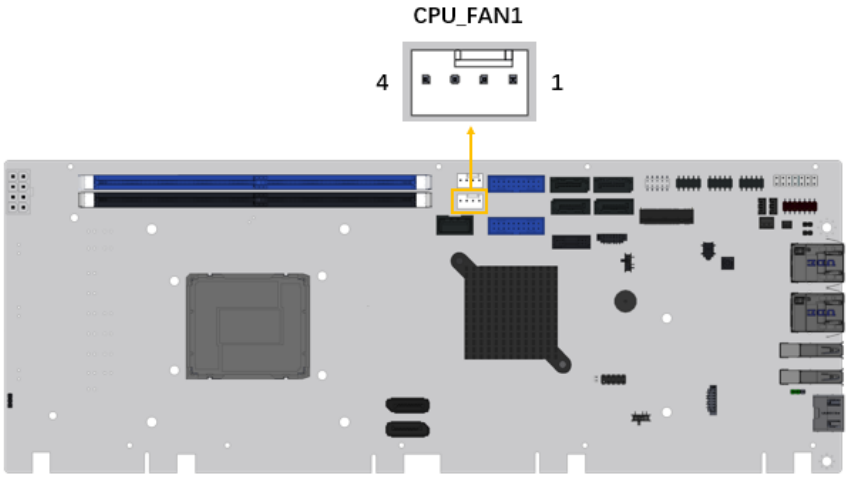


Figure 3-11: CPU Fan Connector Location

Pin	Description
1	GND
2	+12V
3	FANIN
4	PWM(+5V)

Table 3-12: CPU Fan Connector Pinouts

3.3.11 Fan Connectors (System)

CN Label: **SYS_FAN1**

CN Type: 4-pin wafer, p=2.54 mm

CN Location: See **Figure 3-12**

CN Pinouts: See **Table 3-13**

The fan connector attaches to a system cooling fan.

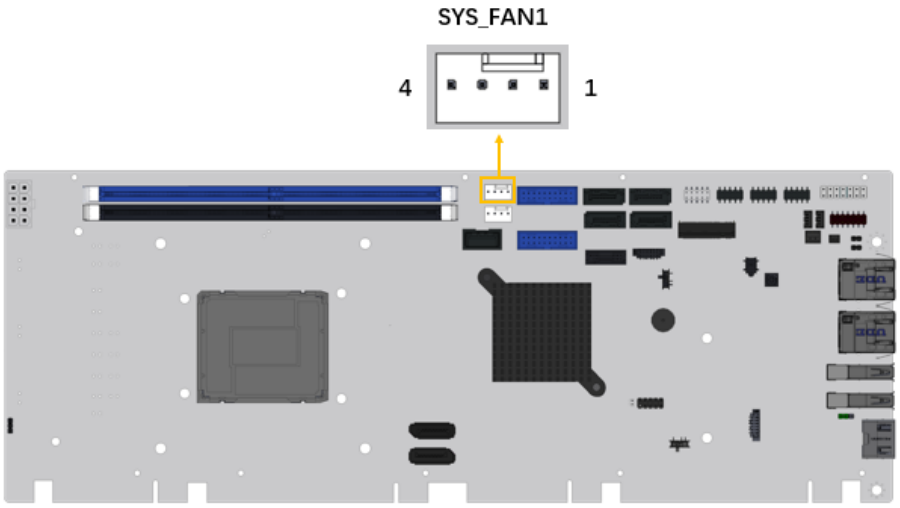


Figure 3-12: System Fan Connector Location

Pin	Description
1	GND
2	+12V
3	FANIN
4	PWM(+5V)

Table 3-13: System Fan (SYS_FAN1) Connector Pinouts

3.3.12 Audio Connector

CN Label: **IAUDIO**

CN Type: 10-pin header, p=2.00 mm

CN Location: See **Figure 3-13**

CN Pinouts: See **Table 3-14**

This connector allows connection to an external audio kit.

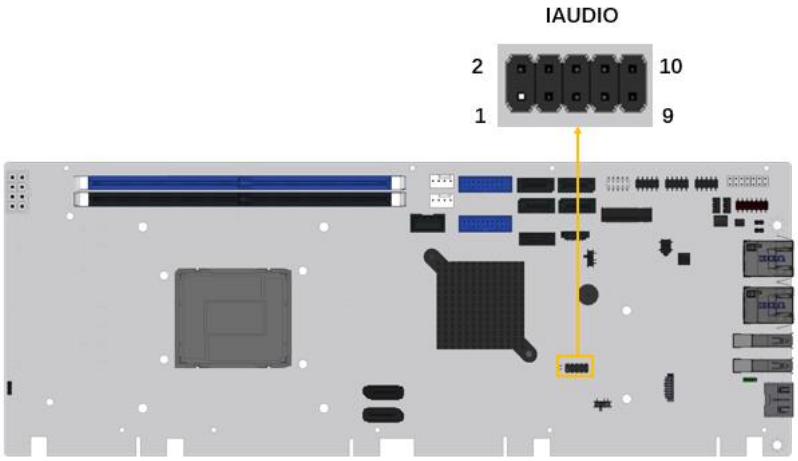


Figure 3-13: Audio Connector Location

Pin	Description	Pin	Description
1	HDA_SYNC_R	2	HDA_BCLK_R
3	HDA_SDO_R	4	HDA_PCBEEPC
5	HDA_SDI_0_R	6	HDA_RST_R
7	+5V	8	GND
9	+12V	10	GND

Table 3-14: Audio Connector Pinouts

3.3.13 Front Panel Connector

CN Label: **F_PANEL1**

CN Type: 14-pin header, p=2.54 mm

CN Location: See **Figure 3-14**

CN Pinouts: See **Table 3-15**

The front panel connector connects to the indicator LEDs and buttons on the computer's front panel.

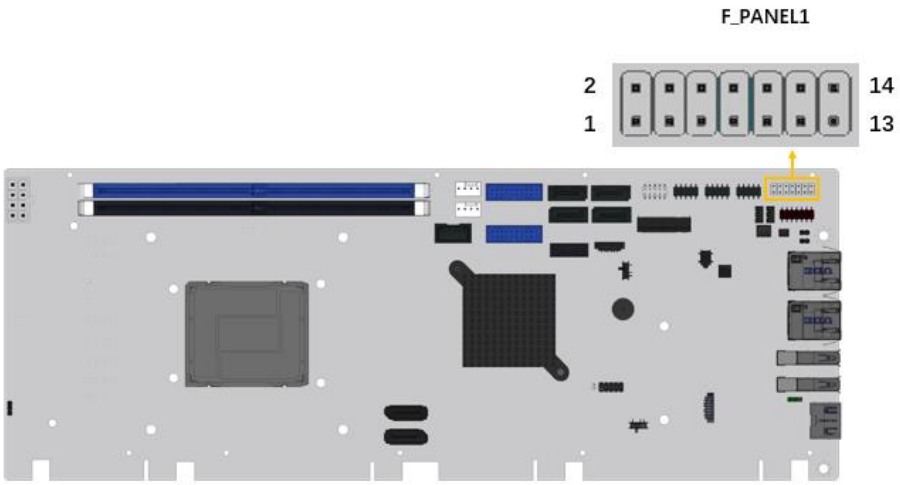


Figure 3-14: Front Panel Connector Location

Function	Pin	Description	Function	Pin	Description
PWR LED	1	+5V	SPKR	2	PC_BEEP_P
	3	NC		4	NC
	5	GND		6	NC-
PWR BTN	7	PWR_BTN_N		8	PC_BEEP_N
	9	GND		10	NC
HDD LED	11	HD_LED_P	RESET	12	PM_SYSRST_N
	13	HD_LED_N		14	GND

Table 3-15: Front Panel Connector Pinouts

3.3.14 I²C Connector

CN Label: **J_I2C1**

CN Type: 4-pin wafer, p=1.25 mm

CN Location: See **Figure 3-15**

CN Pinouts: See **Table 3-16**

The I²C connector is used to connect I²C-bus devices to the motherboard.

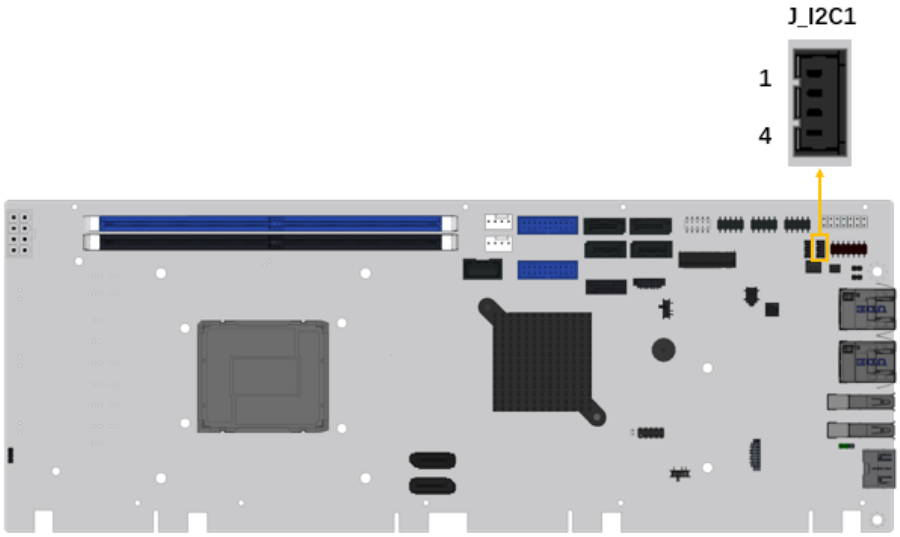


Figure 3-15: I²C Connector Location

Pin	Description
1	GND
2	SMDAT0_EC
3	SMCLK0_EC
4	+5V

Table 3-16: I²C Connector Pinouts

3.3.15 SMBus Connector

CN Label: **J_SMB1**

CN Type: 4-pin wafer, p=1.25 mm

CN Location: See **Figure 3-16**

CN Pinouts: See **Table 3-17**

The SMBus (System Management Bus) connector provides low-speed system management communications.

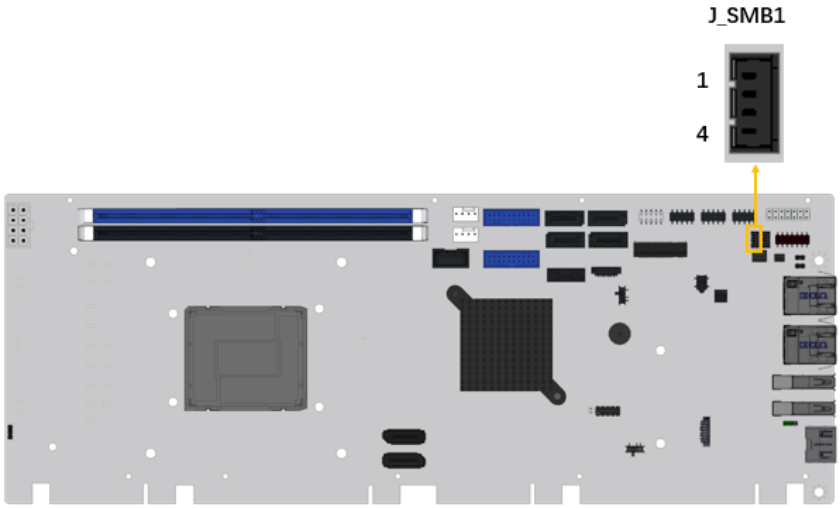


Figure 3-16: SMBus Connector Location

Pin	Description
1	GND
2	SMB_DATA_MAIN
3	SMB_CLK_MAIN
4	+5V

Table 3-17: SMBus Connector Pinouts

3.3.16 LAN Link LED Connector

CN Label: **JLAN_LED1, JLAN_LED2**

CN Type: 2-pin header, p=2.00 mm

CN Location: See **Figure 3-17**

CN Pinouts: See **Table 3-18**

The LAN LED connectors are used to connect to the LAN LED indicators on the chassis to indicate users the link activities of the two LAN ports.

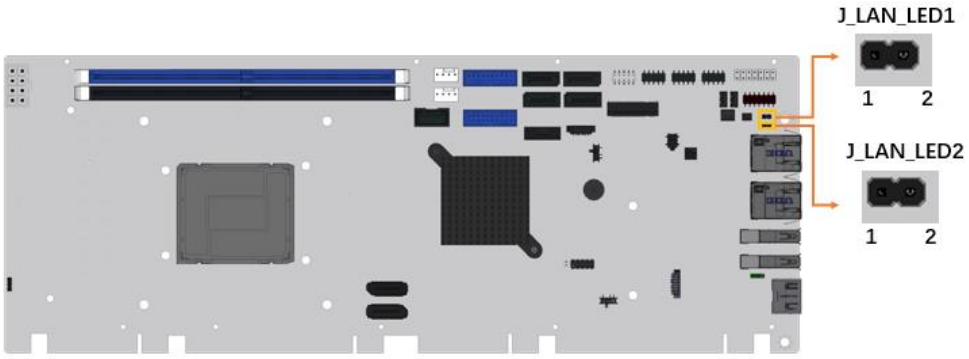


Figure 3-17: LAN LED Connector Locations

Pin	Description
1	+3.3V
2	LAN_LED_LINK#_ACT

Table 3-18: LAN LED Connector Pinouts

3.3.17 M.2 M-key slot

CN Label: **M2_M1**

CN Type: M-key slot

CN Location: See **Figure 3-18**

CN Pinouts: See **Table 3-19**

The M.2 2242/2280 slot is keyed in the M position.

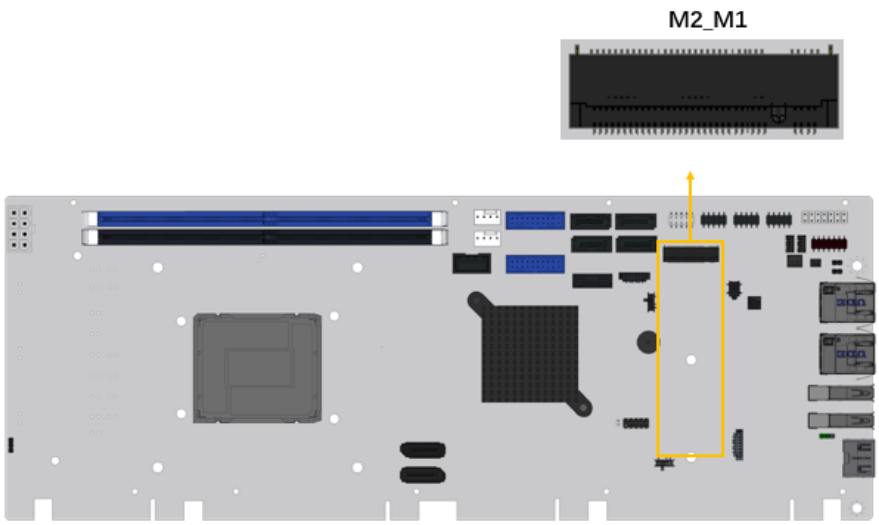


Figure 3-18: M.2 M-key ((2242/2280) Slot Location

Pin	Description	Pin	Description
1	GND	2	+3.3V
3	GND	4	+3.3V
5	PCIE_20_RX_DN	6	N/C
7	PCIE_20_RX_DP	8	N/C
9	GND	10	NGFF1_ACT_N
11	PCIE_TX_DN20	12	+3.3V
13	PCIE_TX_DP20	14	+3.3V
15	GND	16	+3.3V
17	PCIE_19_RX_DN	18	+3.3V
19	PCIE_19_RX_DP	20	N/C

Pin	Description	Pin	Description
21	GND	22	N/C
23	PCIE_TX_DN19	24	N/C
25	PCIE_TX_DP19	26	N/C
27	GND	28	N/C
29	PCIE_18_RX_DN	30	N/C
31	PCIE_18_RX_DP	32	N/C
33	GND	34	N/C
35	PCIE_TX_DN18	36	N/C
37	PCIE_TX_DP18	38	M_2_SSD_SLP
39	GND	40	N/C
41	PCIE_17_RX_DN	42	N/C
43	PCIE_17_RX_DP	44	N/C
45	GND	46	N/C
47	PCIE_TX_DN17	48	N/C
49	PCIE_TX_DP17	50	PLT_RST_N
51	GND	52	SRCCLKREQB_17 _N
53	PCIE_CLK_DN17	54	NC
55	PCIE_CLK_DP17	56	N/C
57	GND	58	N/C
59	N/C	60	N/C
61	N/C	62	N/C
63	N/C	64	N/C
65	N/C	66	N/C
67	N/C	68	NC
69	N/C	70	+3.3V
71	GND	72	+3.3V
73	GND	74	+3.3V
75	GND		

Table 3-19: M.2 M-key ((2242/2280) Slot Pinouts

3.3.18 On-Board Power Switch

CN Label: **PWR_SW1**

CN Type: Push button

CN Location: See **Figure 3-19**

The on-board power button controls system power.

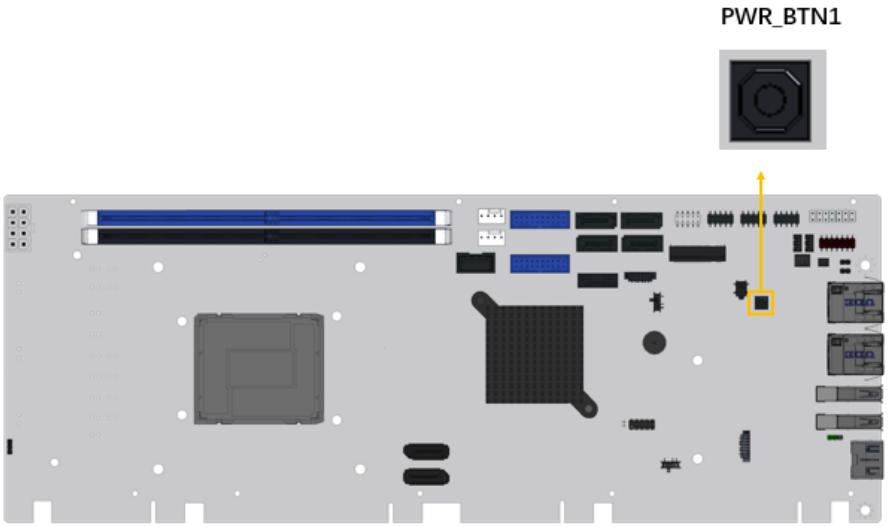


Figure 3-19: Power Button Location

3.3.19 DDR5 DIMM Slots

CN Label: **DIMM1, DIMM3**

CN Type: 288-pin DDR4 DIMM socket

CN Location: See **Figure 3-20**

The DIMM sockets are for DDR5 DIMM memory modules.

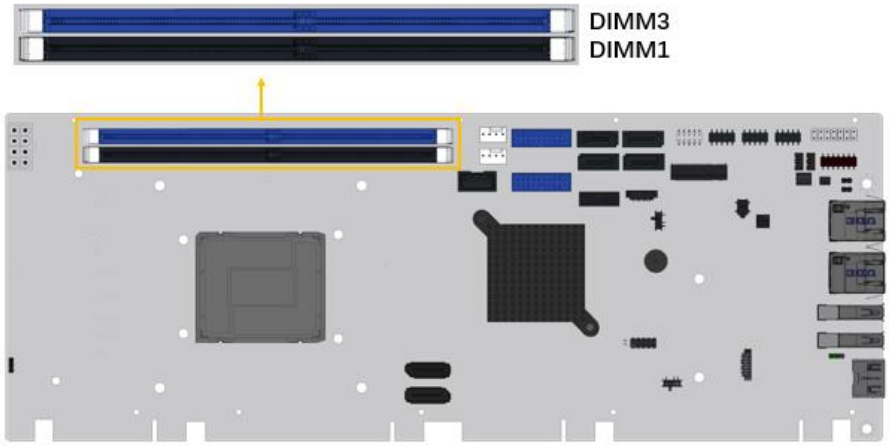


Figure 3-20: DDR5 DIMM Socket Locations

3.3.20 SATA 6Gb/s Connectors

CN Label: **SATA1, SATA2, SATA3, SATA4**

CN Type: 7-pin SATA connector

CN Location: See **Figure 3-21**

CN Pinouts: See **Table 3-20**

The SATA drive connectors can be connected to SATA drives and support up to 6Gb/s data transfer rate.

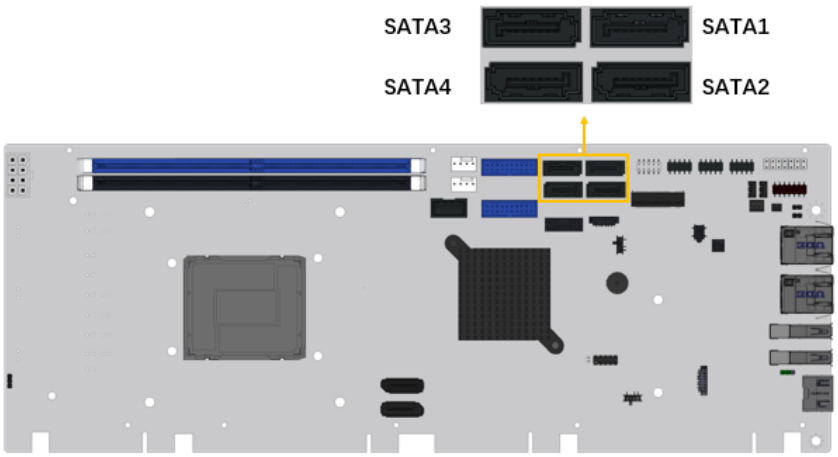


Figure 3-21: SATA 6Gb/s Connector Locations

Pin	Description
1	GND
2	SATA_TXP
3	SATA_TXN
4	GND
5	SATA_RXN
6	SATA_RXP
7	GND
8	NC
9	NC

Table 3-20: SATA 6Gb/s Connector Pinouts

3.3.21 RS-232 Serial Port Connectors

CN Label: **COM3, COM4**

CN Type: 10-pin header, p=2.00 mm

CN Location: See **Figure 3-22**

CN Pinouts: See **Table 3-21**

Each of these connectors provides RS-232 connections.

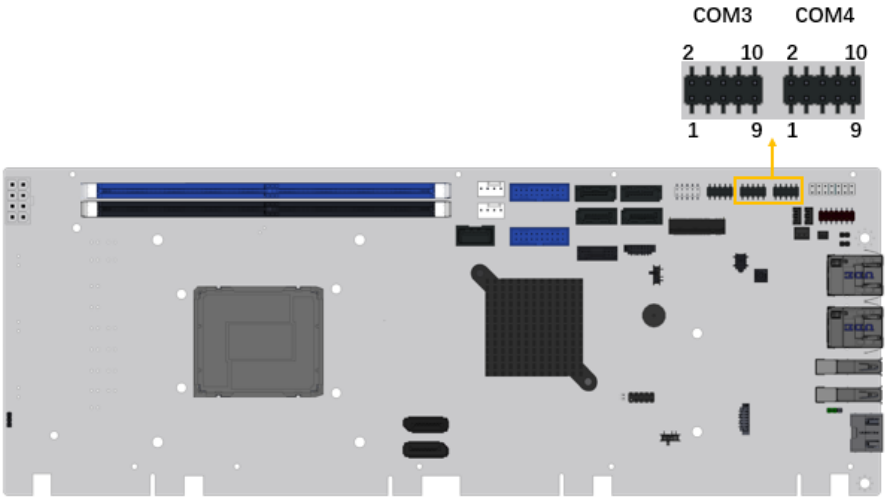


Figure 3-22: RS-232 Serial Port Connector Location

Pin	Description	Pin	Description
1	DATA CARRIER DETECT(DCD)	2	DATA SET READY (DSR)
3	RECEIVE DATA (RXD)	4	REQUEST TO SEND (RTS)
5	TRANSMIT DATA (TXD)	6	CLEAR TO SEND (CTS)
7	DATA TERMINAL READY (DTR)	8	RING INDICATOR (RI)
9	GND	10	GND

Table 3-21: RS-232 Serial Port Connector Pinouts

3.3.22 RS-232/422/485 Serial Port Connectors

CN Label: **COM1, COM2**

CN Type: 10-pin header, p=2.00 mm

CN Location: See **Figure 3-23**

CN Pinouts: See **Table 3-22**

Each of these connectors provides RS-422 or RS-485 communications.

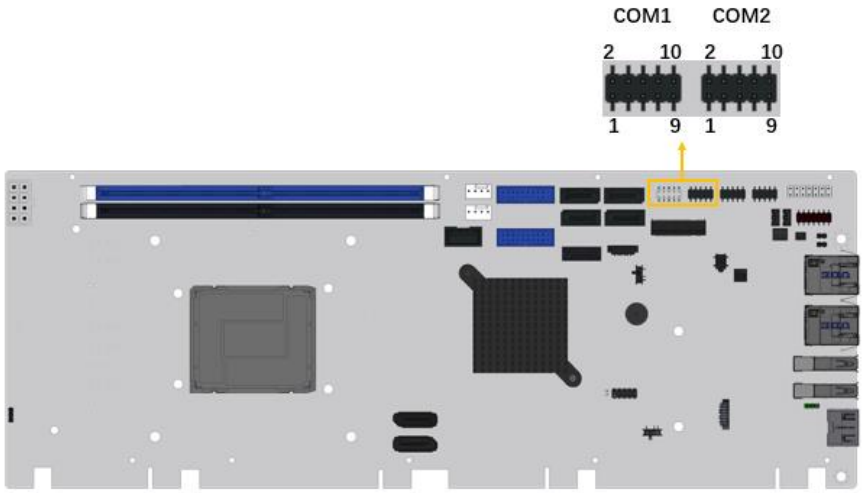


Figure 3-23: RS-232/422/485 Serial Port Connectors Location

PIN	RS-232	RS-422	RS-485
1	DCD	TXD422-	TXD485-
2	DSR	TXD422+	TXD485+
3	RX	RXD422+	--
4	RTS	RXD422-	--
5	TX	--	--
6	CTS	--	--
7	DTR	--	--
8	RI	--	--
9	RI	--	--

Table 3-22: RS-232/422/485 Serial Port Connectors Pinouts

3.3.23 Flash SPI ROM Connector

CN Label: **JSPI1**

CN Type: 6-pin wafer, p=1.25 mm

CN Location: See **Figure 3-24**

CN Pinouts: See **Table 3-23**

The Flash SPI ROM connector is used to flash the SPI ROM.

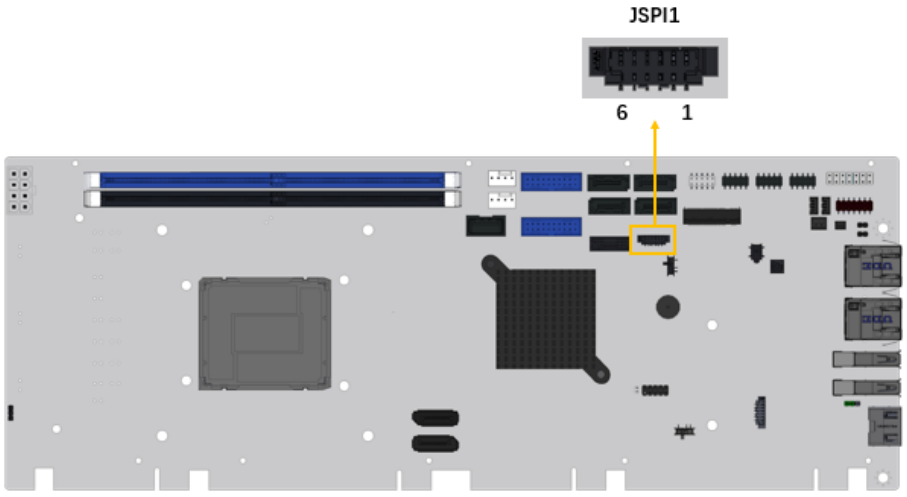


Figure 3-24: Flash SPI ROM Connector Location

Pin	Description	Pin	Description
1	+V3.3M_SPI_CON	4	SPI_CLK_SW
2	SPI_CS	5	SPI_SI_SW
3	SPI_SO_SW	6	GND

Table 3-23: Flash SPI ROM Connector Pinouts

3.3.24 Internal USB 3.2 Gen 1 Connector

CN Label: **JUSB3_5, JUSB3_4**

CN Type: 20-pin box header, p=2.00 mm

CN Location: See **Figure 3-25**

CN Pinouts: See **Table 3-24**

The JUSB3_5, JUSB3_4 provides USB 3.2 Gen 1 (5Gb/s) ports.

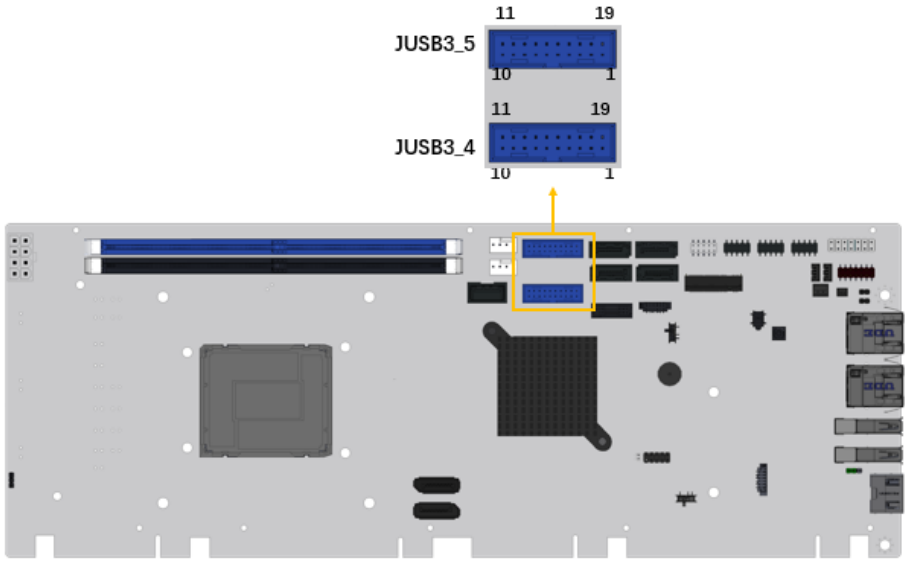


Figure 3-25: Internal USB 3.2 Gen 1 Connector Location

Pin	Description	Pin	Description
1	VCC1	11	SBD1+
2	USB3_RX1_DN	12	SBD1-
3	USB3_RX1_dP	13	GND
4	GND	14	USB3_TX2_DP
5	USB3_TX1_DN	15	USB3_TX2_DN
6	USB3_TX1_PD	16	GND
7	GND	17	USB3_RX2_DP
8	SBD0-	18	USB3_RX2_DN

Pin	Description	Pin	Description
9	SBD0+	19	VCC2
10	N/C		

Table 3-24: Internal USB 3.2 Gen 1 Connector Pinouts

3.3.25 Internal USB 3.2 Gen 2 Connector (Type-A)

CN Label: **USB3_3**

CN Type: USB 3.2 Gen 2 Type-A Port

CN Location: See **Figure 3-26**

The Internal USB 3.2 Gen 1 connector connects to USB 3.2 devices. This connector provides USB 3.2 Gen 1 (10Gb/s) ports.

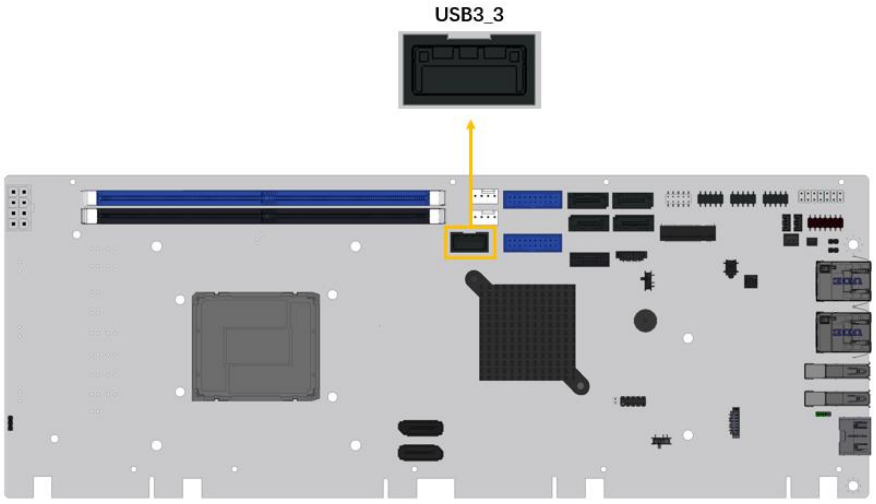


Figure 3-26: Internal USB 3.2 Gen 2 Connector Location

3.3.26 Internal DP Connector

CN Label: **DP1, DP2**

CN Type: DisplayPort

CN Location: See **Figure 3-27**

The DP1 connector connects to a display device with DisplayPort interface. DP2 is not plugged into the DisplayPort interface, but it can be an option. If needed, MOQ100.

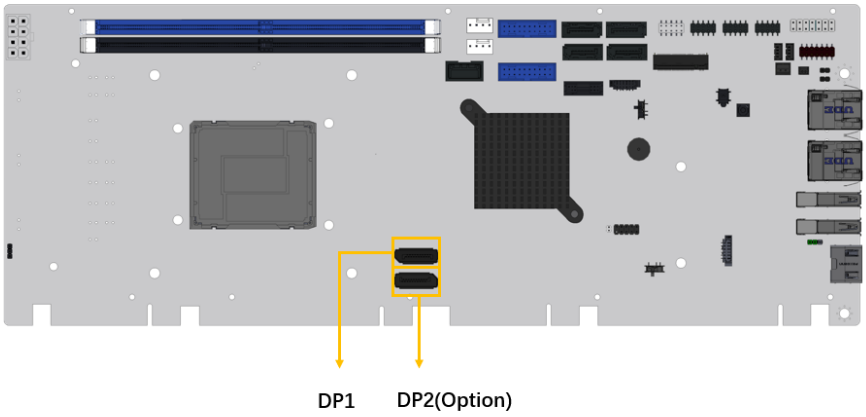


Figure 3-27: Internal DP Connector Location

3.4 External Peripheral Interface Connector Panel

The figure below shows the external peripheral interface connector (EPIC) panel. The EPIC panel consists of the following:

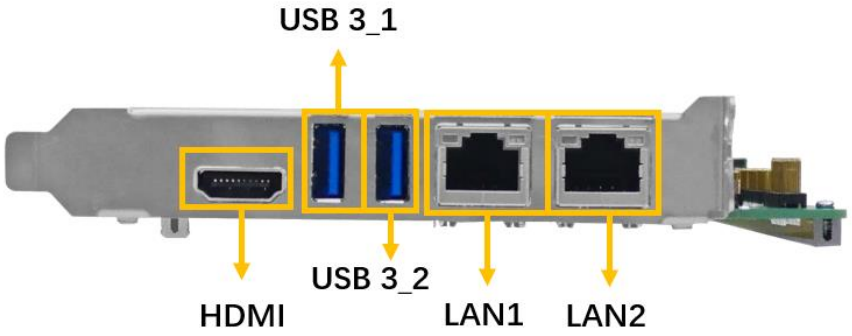


Figure 3-28: External Peripheral Interface Connector

3.4.1 External 2.5GbE RJ-45 Connectors

CN Label: **LAN1, LAN2**

CN Type: RJ-45

CN Location: See **Figure 3-29**

CN Pinouts: See **Table 3-25**

Each LAN connector connects to a local network.

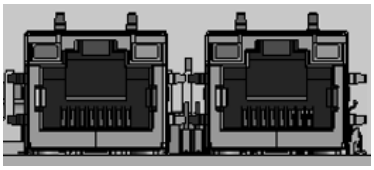


Figure 3-29: LAN Location

LED	Description	LED	Description
A	on: linked blinking: data is being sent/received-	B	off: 100 Mb/s orange: 1000 Mb/s green: 2500 Mb/s

Table 3-25: LAN LED Pinouts

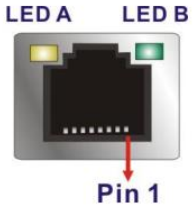


Figure 3-30: LAN LED Location

3.4.2 External HDMI Connector

CN Label: **HDMI**

CN Type: HDMI connector

CN Location: See **Figure 3-31**

CN Pinouts: See **Table 3-26**

The HDMI connector can connect to an HDMI device.

Pin	Description	Pin	Description
1	HDMI_DATA2	11	GND
2	GND	12	HDMI_CLK#
3	HDMI_DATA2#	13	N/C
4	HDMI_DATA1	14	N/C
5	GND	15	HDMI_SCL
6	HDMI_DATA1#	16	HDMI_SDA
7	HDMI_DATA0	17	GND
8	GND	18	+5V
9	HDMI_DATA0#	19	HDMI_HPD
10	HDMI_CLK		

Table 3-26: HDMI Connector Pinouts

Figure 3-31: HDMI Connector

3.4.3 External USB 3.2 Gen 2 Connectors (Type-A)

CN Label: **USB3_1, USB3_2**

CN Type: USB 3.2 Gen 2 Type A

CN Location: See **Figure 3-32**

CN Pinouts: See **Table 3-27**

The pinouts of USB 3.2 Gen 2 connectors are shown below.

PIN	DESCRIPTION	PIN	DESCRIPTION
1	SB3_PWR1	6	USB3_RX1_P
2	USB_D1N	7	GND
3	USB_D1P	8	USB3_TX1_N
4	GND	9	USB3_TX1_P
5	USB3_RX1_N		

Table 3-27: External USB 3.2 Gen 2 Connectors (Type-A) Pinouts

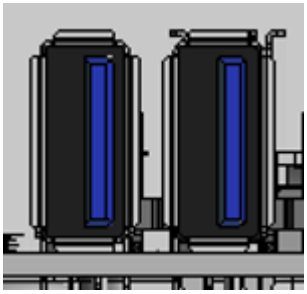


Figure 3-32: USB 3.2 Gen2 Connectors (Type-A)

Chapter

4

Installation

4.1 Anti-static Precautions

WARNING:

Failure to take ESD precautions during the installation of the PCIE-RPL-Q670 may result in permanent damage to the PCIE-RPL-Q670 and severe injury to the user.

Electrostatic discharge (ESD) can cause serious damage to electronic components, including the PCIE-RPL-Q670. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the PCIE-RPL-Q670 or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- ***Wear an anti-static wristband***: Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- ***Self-grounding***: Before handling the board touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- ***Use an anti-static pad***: When configuring the PCIE-RPL-Q670, place it on an anti-static pad. This reduces the possibility of ESD damaging the PCIE-RPL-Q670.
- ***Only handle the edges of the PCB***: When handling the PCB, hold the PCB by the edges.

4.2 Internal Peripheral Device Connections

This section outlines the installation of peripheral devices to the onboard connectors.

4.2.1 SATA Drive Connection

The PCIE-RPL-Q670 is shipped with two SATA drive cables. To connect the SATA drives to the connectors, please follow the steps below.

Step 1: **Locate the connectors**. The locations of the SATA drive connectors are shown in **Chapter 3**.

Step 2: **Insert the cable connector**. Insert the cable connector into the on-board SATA drive connector until it clips into place. See **Figure 4-1**.

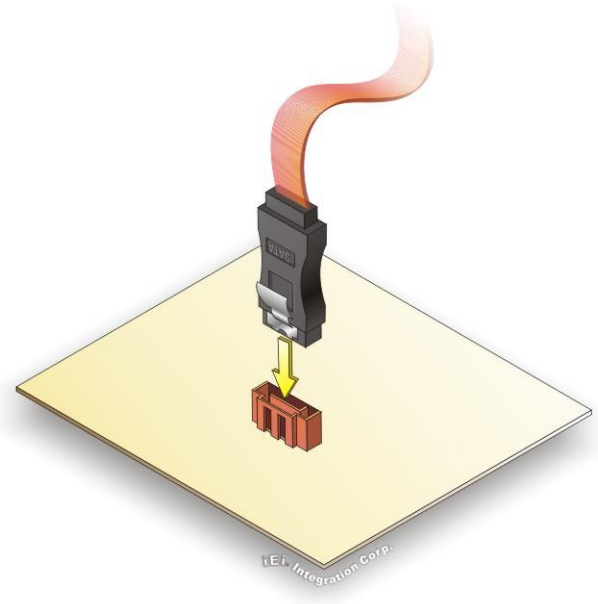


Figure 4-1: SATA Drive Cable Connection

Step 3: **Connect the cable to the SATA disk**. Connect the connector on the other end of the cable to the connector at the back of the SATA drive. See **Figure 4-2**.

Step 4: **Connect the SATA power cable**. Connect the SATA power connector to the back of the SATA drive. See **Figure 4-2**.

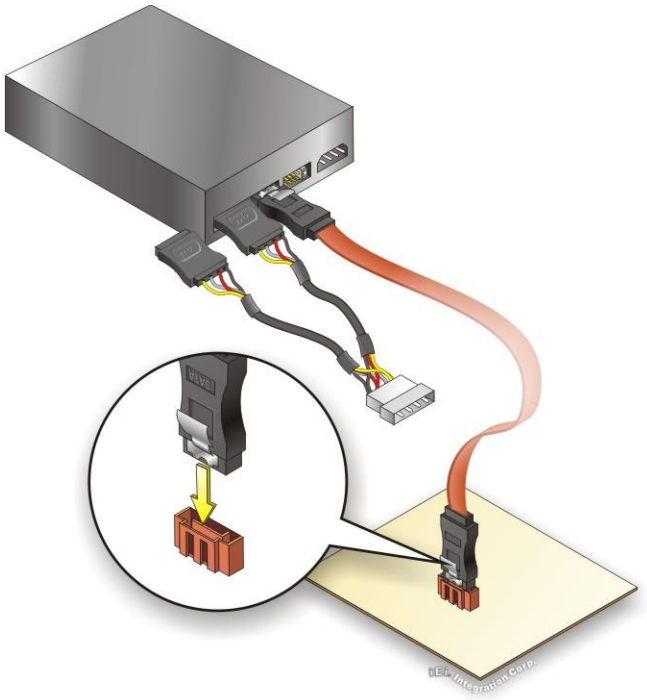


Figure 4-2: SATA Power Drive Connection

The SATA power cable can be bought from IEI. See Optional Items in Section 2.4.

4.3 Installation Considerations

NOTE:

The following installation notices and installation considerations should be read and understood before installation. All installation notices must be strictly adhered to. Failing to adhere to these precautions may lead to severe damage and injury to the person performing the installation.

WARNING:

The installation instructions described in this manual should be carefully followed in order to prevent damage to the components and injury to the user.

Before and during the installation please **DO** the following:

- Read the user manual:
  - The user manual provides a complete description of the PCIE-RPL-Q670 installation instructions and configuration options.
- Wear an electrostatic discharge cuff (ESD):
  - Electronic components are easily damaged by ESD. Wearing an ESD cuff removes ESD from the body and helps prevent ESD damage.
- Place the PCIE-RPL-Q670 on an anti-static pad:
  - When installing or configuring the motherboard, place it on an anti-static pad. This helps to prevent potential ESD damage.
- Turn all power to the PCIE-RPL-Q670 off:
  - When working with the PCIE-RPL-Q670, make sure that it is disconnected from all power supplies and that no electricity is being fed into the system.

Before and during the installation of the PCIE-RPL-Q670, **DO NOT:**

- Remove any of the stickers on the PCB board. These stickers are required for warranty validation.
- Use the product before verifying all the cables and power connectors are properly connected.
- Allow screws to come in contact with the PCB circuit, connector pins, or its components.

4.4 Socket LGA1700 CPU Installation

WARNING:

CPUs are expensive and sensitive components. When installing the CPU please be careful not to damage it in anyway. Make sure the CPU is installed properly and ensure the correct cooling kit is properly installed.

DO NOT touch the pins at the bottom of the CPU. When handling the CPU, only hold it on the sides.

To install the CPU, follow the steps below.

Step 1: **Disengage the load lever** by pressing the lever down and slightly outward to clear the retention tab. Fully open the lever. See **Figure 4-3.**

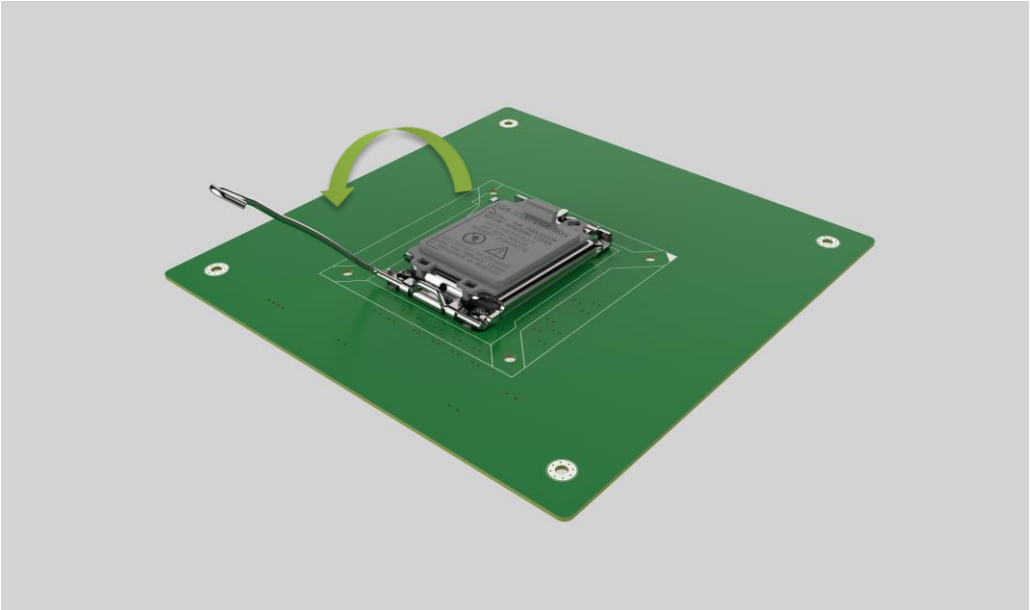


Figure 4-3: Disengage the CPU Socket Load Lever

Step 2: **Open the socket and remove the protective cover.** The black protective cover can be removed by pulling up on the tab labeled "Remove". See **Figure 4-4**.

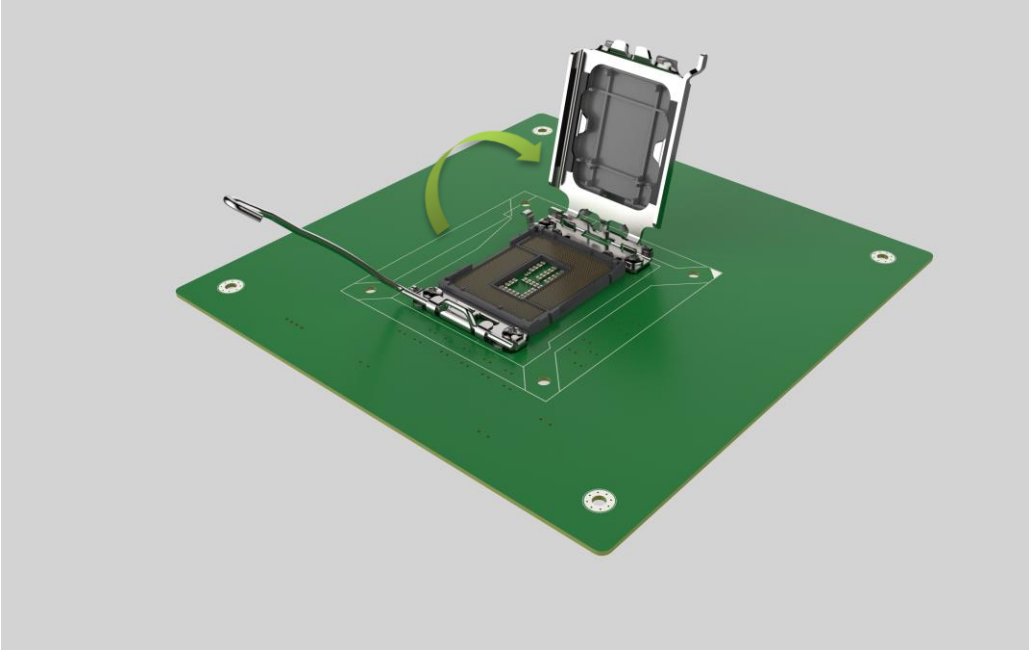


Figure 4-4: Remove Protective Cover

Step 3: **Inspect the CPU socket.** Make sure there are no bent pins and make sure the socket contacts are free of foreign material. If any debris is found, remove it with compressed air.

Step 4: **Orientate the CPU properly.** The contact array should be facing the CPU socket.

WARNING:

DO NOT touch the pins at the bottom of the CPU. When handling the CPU, only hold it on the sides.

Step 5: **Correctly position the CPU.** Match the Pin 1 mark with the cut edge on the CPU socket.

Step 6: **Align the CPU pins.** Locate pin 1 and the two orientation notches on the CPU. Carefully match the two orientation notches on the CPU with the socket alignment keys.

Step 7: **Insert the CPU.** Gently insert the CPU into the socket. If the CPU pins are properly aligned, the CPU should slide into the CPU socket smoothly. See **Figure 4-5.**

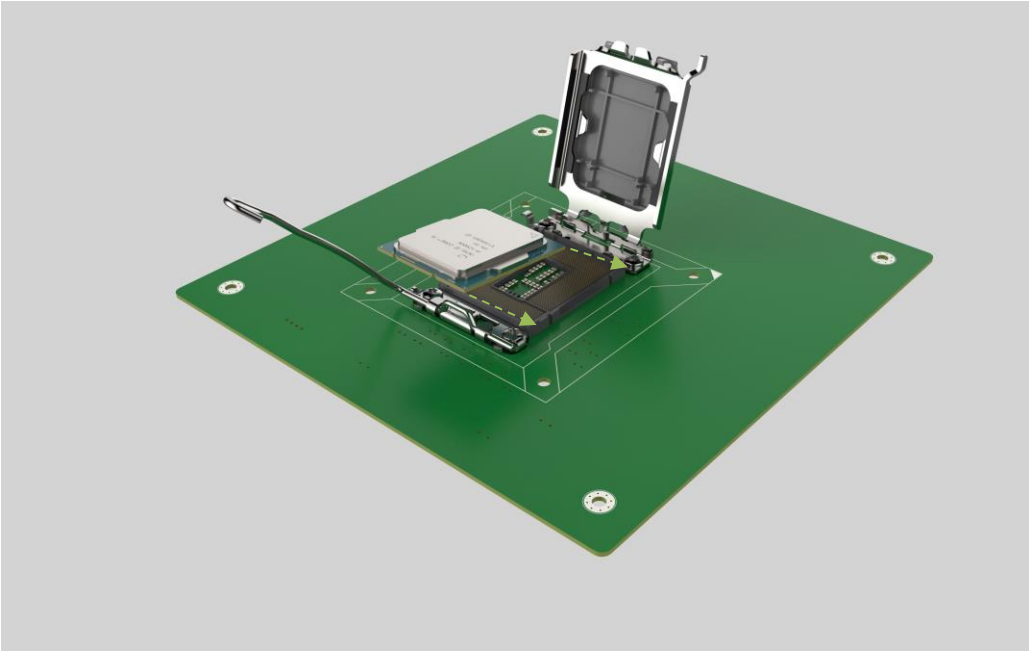


Figure 4-5: Insert the Socket LGA1700 CPU

Step 8: **Close the CPU socket.** Close the load plate and pull the load lever back a little to have the load plate be able to secure to the knob. Engage the load lever by pushing it back to its original position (**Figure 4-6**). There will be some resistance, but will not require extreme pressure.

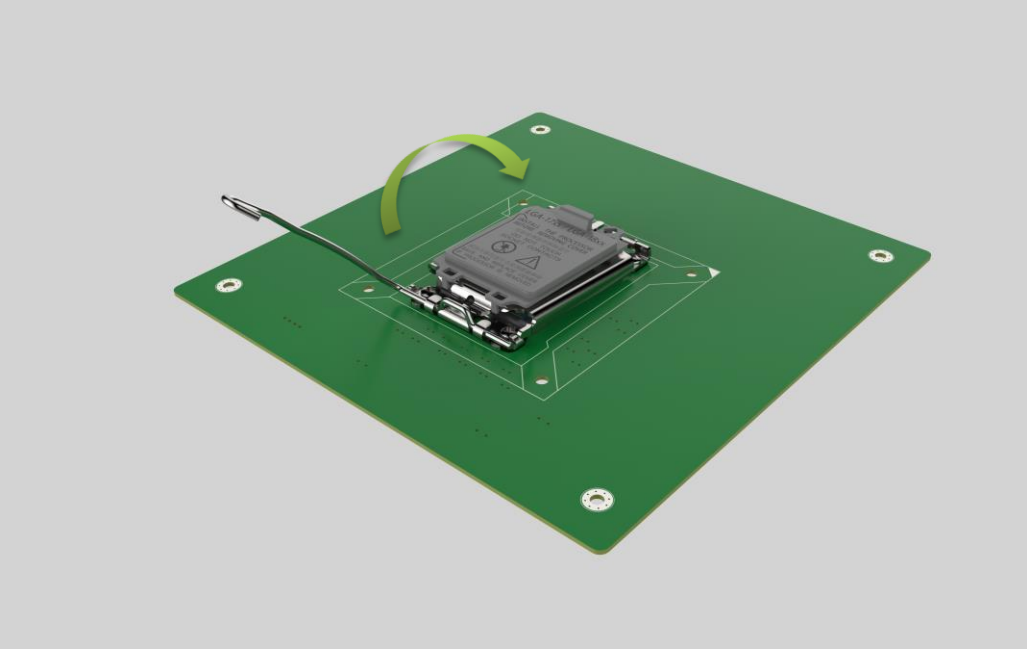


Figure 4-6: Close the Socket LGA1700

Step 9: **Connect the 12 V power to the board.** Connect the 12 V power from the power supply to the board.

4.5 Socket LGA1700 Cooling Kit Installation

WARNING:

DO NOT attempt to install a push-pin cooling fan.

The pre-installed support bracket prevents the board from bending and is ONLY compatible with captive screw type cooling fans.

The cooling kit can be bought from IEI. The cooling kit has a heat sink and fan.

WARNING:

Do not wipe off (accidentally or otherwise) the pre-sprayed layer of thermal paste on the bottom of the heat sink. The thermal paste between the CPU and the heat sink is important for optimum heat dissipation.

To install the cooling kit, follow the instructions below.

Step 1: A cooling kit bracket is pre-installed on the rear of the motherboard. See **Figure 4-7.**

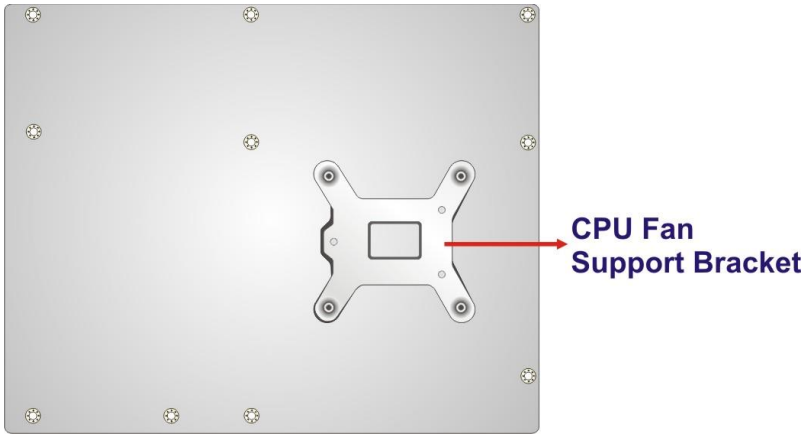


Figure 4-7: Cooling Kit Support Bracket

Step 2: **Place the cooling kit onto the socket LGA1700 CPU**. Make sure the CPU cable can be properly routed when the cooling kit is installed.

Step 3: **Mount the cooling kit**. Gently place the cooling kit on top of the CPU. Make sure the four threaded screws on the corners of the cooling kit properly pass through the holes of the cooling kit bracket.

Step 4: **Tighten the screws**. Use a screwdriver to tighten the four screws. In a diagonal pattern, tighten each screw a few turns then move to the next one, until they are all secured. Do not overtighten the screws.

Step 5: **Connect the fan cable**. Connect the cooling kit fan cable to the CPU fan connector on the PCIE-RPL-Q670. Carefully route the cable and avoid heat generating chips and fan blades.

4.6 DIMM Installation

To install a DIMM, please follow the steps below and refer to **Figure 4-8**.

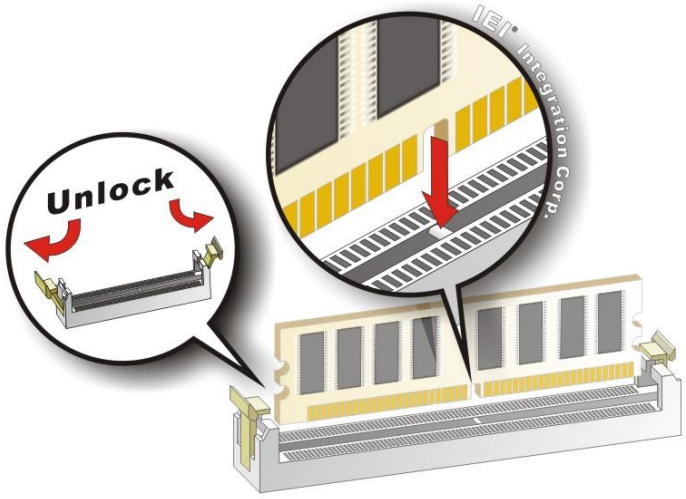


Figure 4-8: DIMM Installation

Step 1: **Open the DIMM socket handles**. Open the two handles outwards as far as they can. See **Figure 4-8**.

Step 2: **Align the DIMM with the socket**. Align the DIMM so the notch on the memory lines up with the notch on the memory socket. See **Figure 4-8**.

Step 3: **Insert the DIMM**. Once aligned, press down until the DIMM is properly seated. Clip the two handles into place. See **Figure 4-8**.

Step 4: **Removing a DIMM**. To remove a DIMM, push both handles outward. The memory module is ejected by a mechanism in the socket.

CAUTION:

For quad channel configuration, install four identical memory modules that feature the same capacity, timings, voltage, number of ranks and the same brand.

4.7 M.2 Module Installation

The PCIE-RPL-Q670 provide two ways to install the M.2 expansion card. One is using screw, and the other is using the retainer. Please follow the steps below.

Mode One: Using screw

Step 1: Locate the M.2 module slot. See **Chapter 3**.

Step 2: Remove the retention screw secured on the motherboard.

Step 3: Line up the notch on the module with the notch on the slot. Slide the M.2 module into the socket at an angle of about 20º (**Figure 4-9)**.

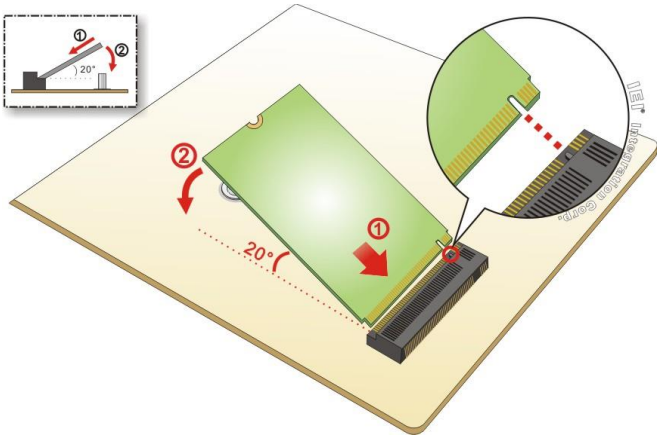


Figure 4-9: Inserting the M.2 Module into the Slot at an Angle

Step 4: Secure the M.2 module with the previously removed retention screw (**Figure 4-10**).

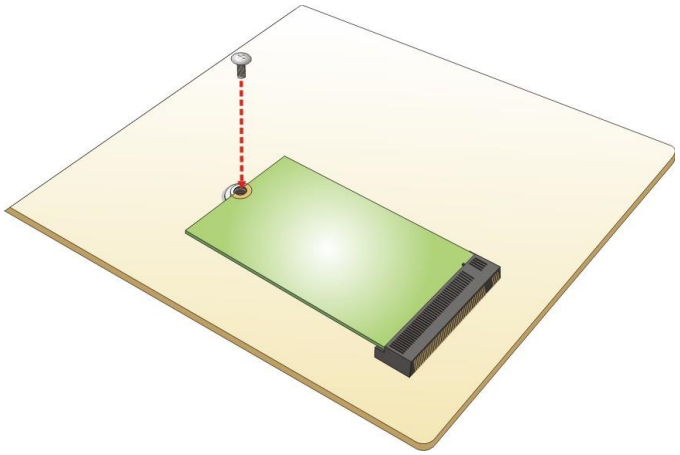


Figure 4-10: Securing the M.2 Module

Mode Two: Using the Retainer

Step 1: Press the retainer down as shown below. (See **Figure 4-11**)

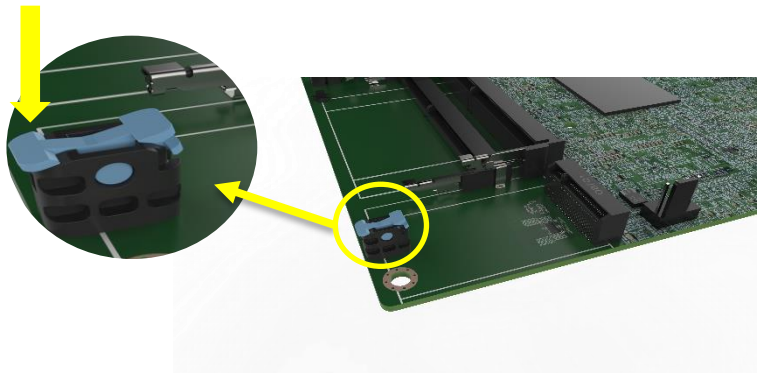


Figure 4-11: Press the Retainer

Step 2: Line up the notch on the M.2 module with the notch on the slot. Slide the M.2 module into the socket at an angle of about 20º. (See **Figure 4-9**)

Step 3: Align the notch on the end of the M.2 module with the clip of the retainer. (See **Figure 4-12**)

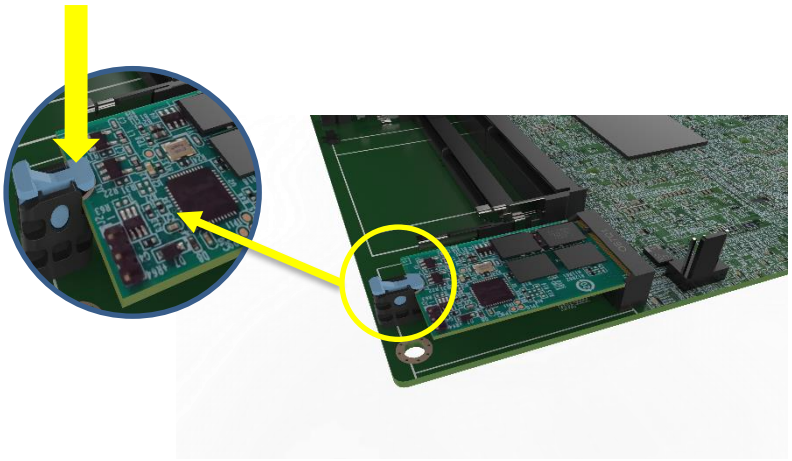


Figure 4-12: Aligning the M.2 Module with the Retainer

Step 4: Press the M.2 module down until it is secured into place by the retainer. (See **Figure 4-13**)

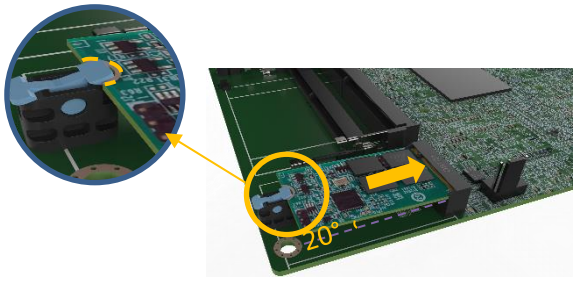


Figure 4-13: Securing the M.2 Module

Step 5: If you want to remove the M.2 module, you should press the retainer down as described in Step 1 to release the M.2 module. (See **Figure 4-11**)

4.8 Software Installation

All the drivers for the PCIE-RPL-Q670 are available on IEI Resource Download Center (https://download.ieiworld.com). Type PCIE-RPL-Q670 and press Enter to find all the relevant software, utilities, and documentation.

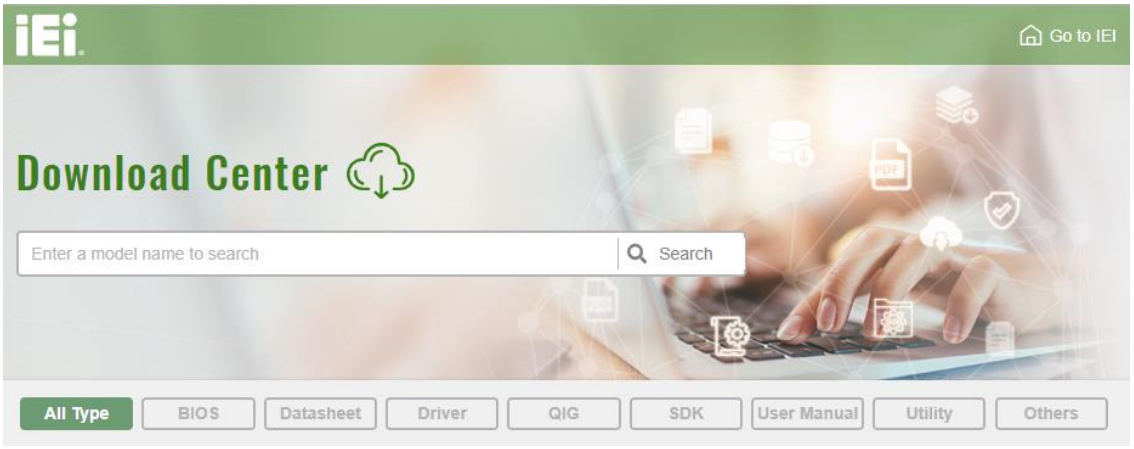
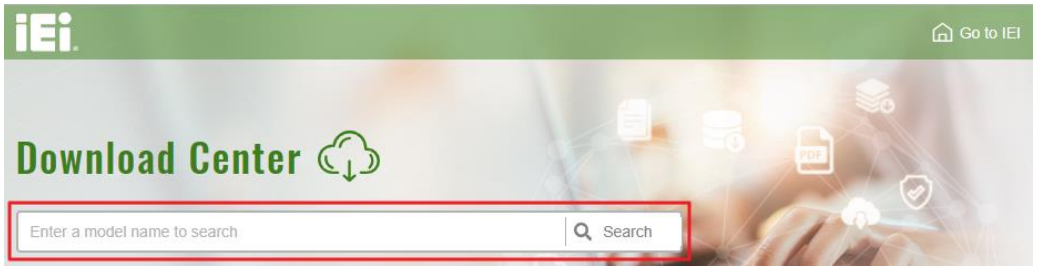


Figure 4-14: IEI Resource Download Center

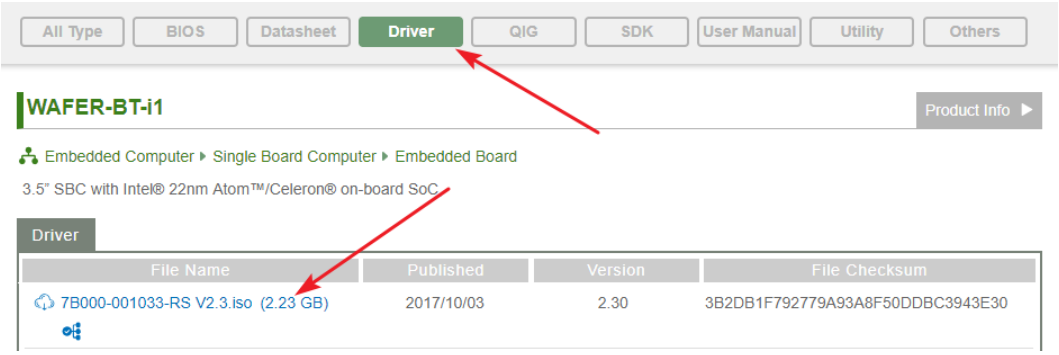
4.9 Driver Download

To download drivers from IEI Resource Download Center, follow the steps below.

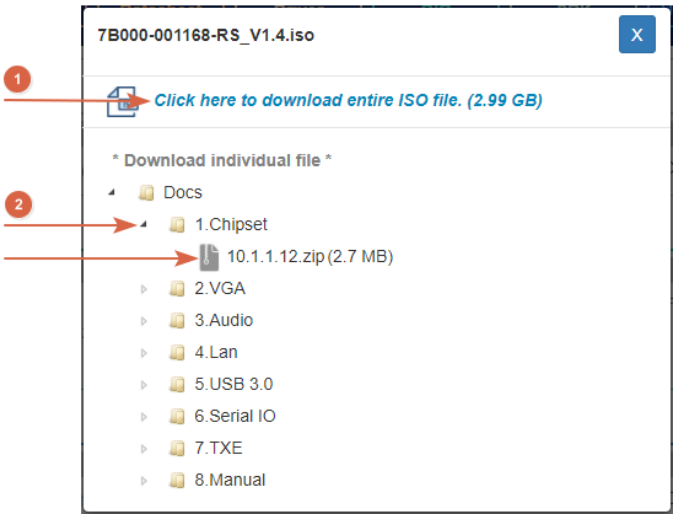
Step 1: Go to https://download.ieiworld.com. Type PCIE-RPL-Q670 and press Enter.



Step 2: All product-related software, utilities, and documentation will be listed. You can choose **Driver** to filter the result.



Step 3: Click the driver file name on the page and you will be prompted with the following window. You can download the entire ISO file (❶), or click the small arrow to find an individual driver and click the file name to download (❷).



NOTE:

To install software from the downloaded ISO image file in Windows 8, 8.1 or 10, double-click the ISO file to mount it as a virtual drive to view its content. On Windows 7 system, an additional tool (such as Virtual CD-ROM Control Panel from Microsoft) is needed to mount the file.

Chapter

5

BIOS

5.1 Introduction

The BIOS is programmed onto the BIOS chip. The BIOS setup program allows changes to certain system settings. This chapter outlines the options that can be changed.

NOTE:

Some of the BIOS options may vary throughout the life cycle of the product and are subject to change without prior notice.

5.1.1 Starting Setup

The UEFI BIOS is activated when the computer is turned on. The setup program can be activated in one of two ways.

1. **Using keyboard**: Press the **DEL** or **F2** as soon as the system is turned on.
2. **Using touchscreen**: Press the **Setup** button on the upper right corner of the BIOS Starting Menu.

If the message disappears before the **DEL or F2** key is pressed, restart the computer and try again, then the BIOS Starting Menu will appear. Select "Setup" and press Enter to get into the BIOS Setup.

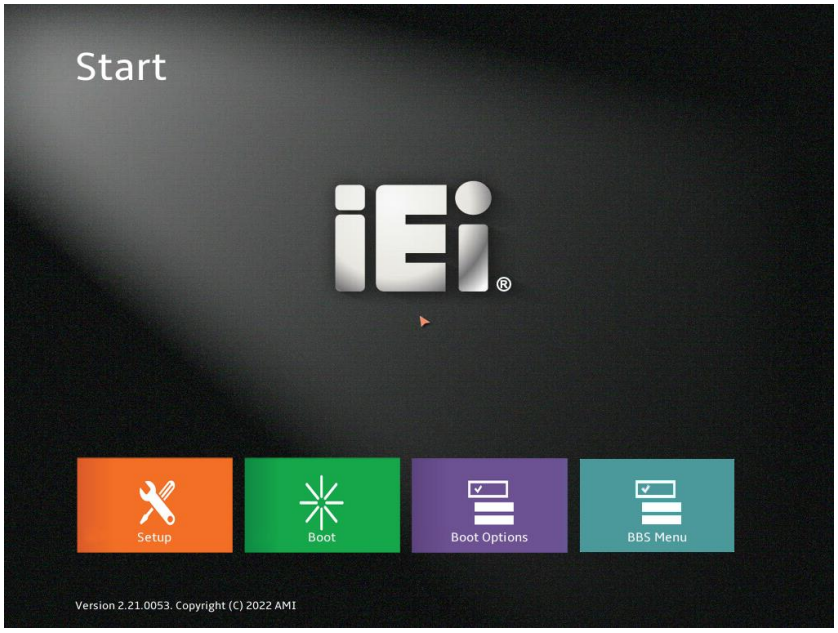


Figure 5-1: BIOS Starting Menu

5.1.2 Using Setup

The BIOS Setup menu can be navigated by using a keyboard or a touchscreen.

5.1.2.1 Keyboard Navigation

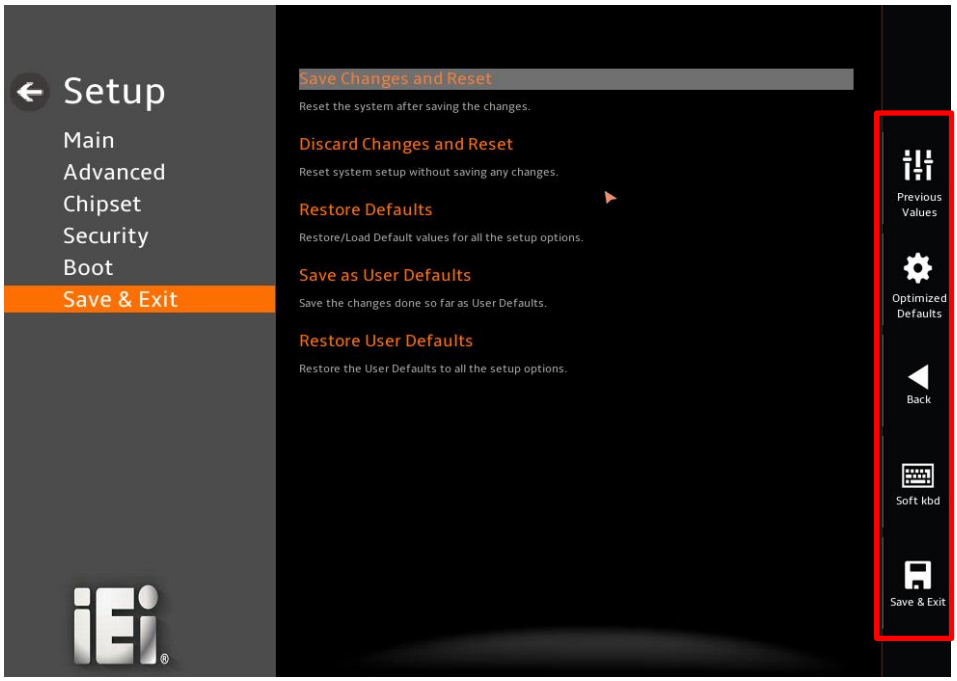
For keyboard navigation, use the navigation keys shown in **Table 5-1**.

Key	Function
Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item on the left hand side
Right arrow	Move to the item on the right hand side
+	Increase the numeric value or make changes
-	Decrease the numeric value or make changes
Page Up	Move to the previous page
Page Dn	Move to the next page
Esc	Main Menu – Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
F1	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2	Load previous values
F3	Load optimized defaults
F4	Save changes and Exit BIOS
<K>	Scroll help area upwards
<M>	Scroll help area downwards

Table 5-1: BIOS Navigation Keys

5.1.2.2 Touch Navigation

For touchscreen navigation, use the on-screen navigation keys shown below.



On-screen Button	Function
Previous Values	Load the last value you set.
Optimized Defaults	Load the factory default values in order to achieve the best performance.
Back	Return to the previous menu.
Soft kbd	Display the on-screen keyboard.
Save & Exit	Save the changes made to the BIOS options and reset the system.

Table 5-2: BIOS On-screen Navigation Keys

5.1.3 Getting Help

When **F1** is pressed a small help window describing the appropriate keys to use and the possible selections for the highlighted item appears. To exit the Help Window, press the **Esc** key.

5.1.4 Unable to Reboot after Configuration Changes

If the computer cannot boot after changes to the system configuration is made, CMOS defaults. Use the clear CMOS button described in **Chapter 4**.

5.1.5 BIOS Menu Bar

The **menu bar** on top of the BIOS screen has the following main items:

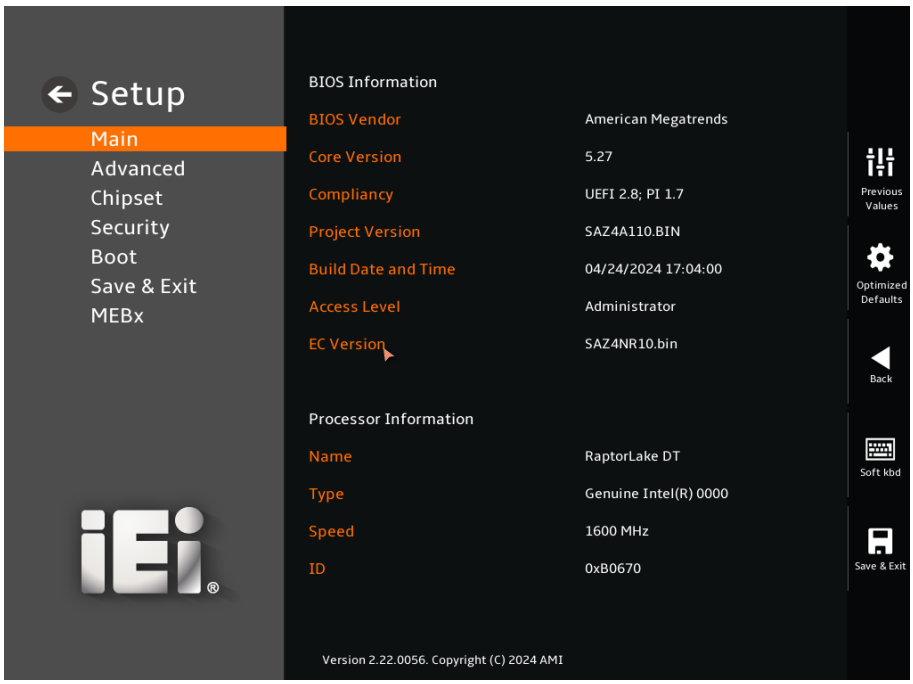
- Main – Changes the basic system configuration.
- Advanced – Changes the advanced system settings.
- Chipset – Changes the chipset settings.
- Security – Sets User and Supervisor Passwords.
- Boot – Changes the system boot configuration.
- Save & Exit – Selects exit options and loads default settings

The following sections completely describe the configuration options found in the menu items at the top of the BIOS screen and listed above.

5.2 Main

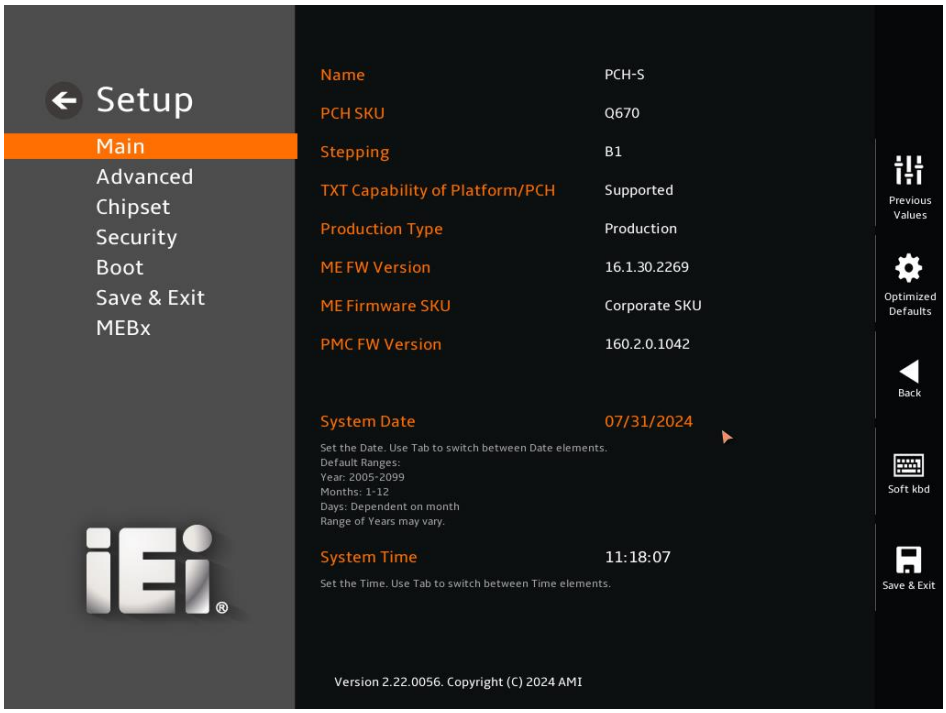
The **Main** BIOS menu (**BIOS Menu 2**) appears when the **BIOS Setup** program is entered.

The **Main** menu gives an overview of the basic system information.



BIOS Menu 1: Main (1/3)

BIOS Menu 2: Main (2/3)



BIOS Menu 3: Main (3/3)

➔ BIOS Information

The **BIOS Information** lists a brief summary of the BIOS. The fields in **BIOS Information** cannot be changed. The items shown in the system overview include:

- **BIOS Vendor:** Installed BIOS vendor
- **Core Version:** Current BIOS version
- **Compliancy:** Current UEFI & PI version
- **Project Version:** the board version
- **Build Date and Time:** Date the current BIOS version was made
- **EC Version:** Current EC version

➔ Processor Information

The **Processor Information** lists a brief summary of the Processor. The fields in **Processor Information** cannot be changed. The items shown in the system overview include:

- **Name:** Displays the Processor Details

- **Type:** Displays the Processor Type
- **Speed:** Displays the Processor Speed
- **ID:** Displays the Processor ID

➔ **PCH Information**

The **PCH Information** lists a brief summary of the PCH. The fields in **PCH Information** cannot be changed. The items shown in the system overview include:

- **Name:** Displays the PCH Name
- **PCH SKU:** Displays the PCH SKU
- **Stepping:** Displays the PCH Stepping
- **TXT Capability of Platform/PCH:** Displays the TXT Capability
- **Production Type:** Displays the Production Type
- **ME FW Version:** Displays the ME Firmware Version
- **ME Firmware SKU:** Displays the ME Firmware SKU
- **PMC FW Version:** Displays the PMC Firmware Version

➔ **System Date [xx/xx/xx]**

Use the **System Date** option to set the system date. Manually enter the day, month and year.

➔ **System Time [xx:xx:xx]**

Use the **System Time** option to set the system time. Manually enter the hours, minutes and seconds.

5.3 Advanced

Use the **Advanced** menu (**BIOS Menu 4**) to configure the CPU and peripheral devices through the following sub-menus:

WARNING!

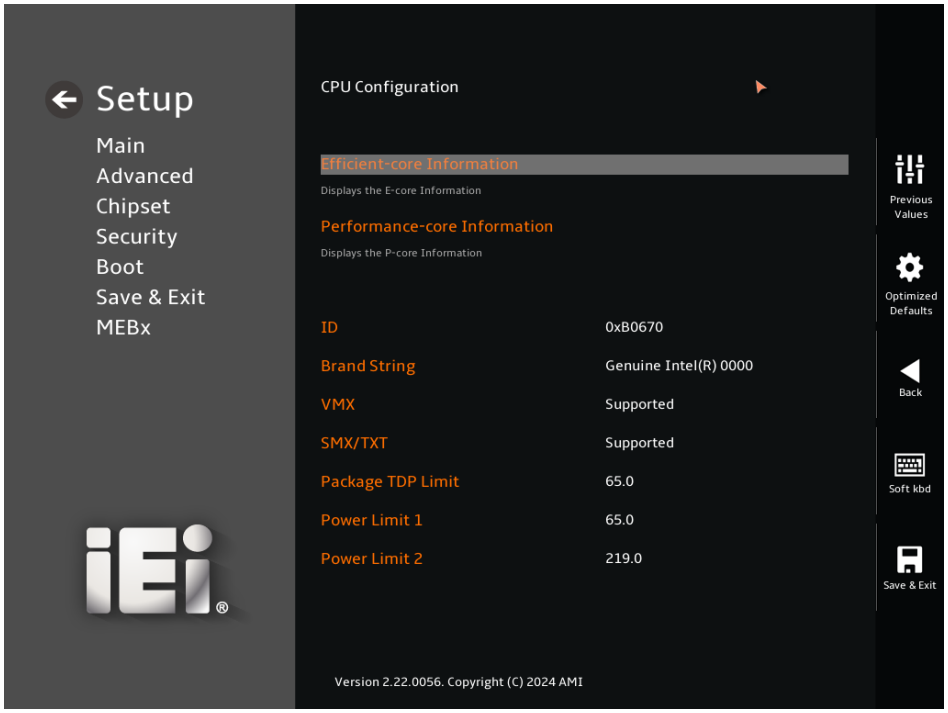
Setting the wrong values in the sections below may cause the system to malfunction. Make sure that the settings made are compatible with the hardware.

BIOS Menu 4: Advanced (1/2)

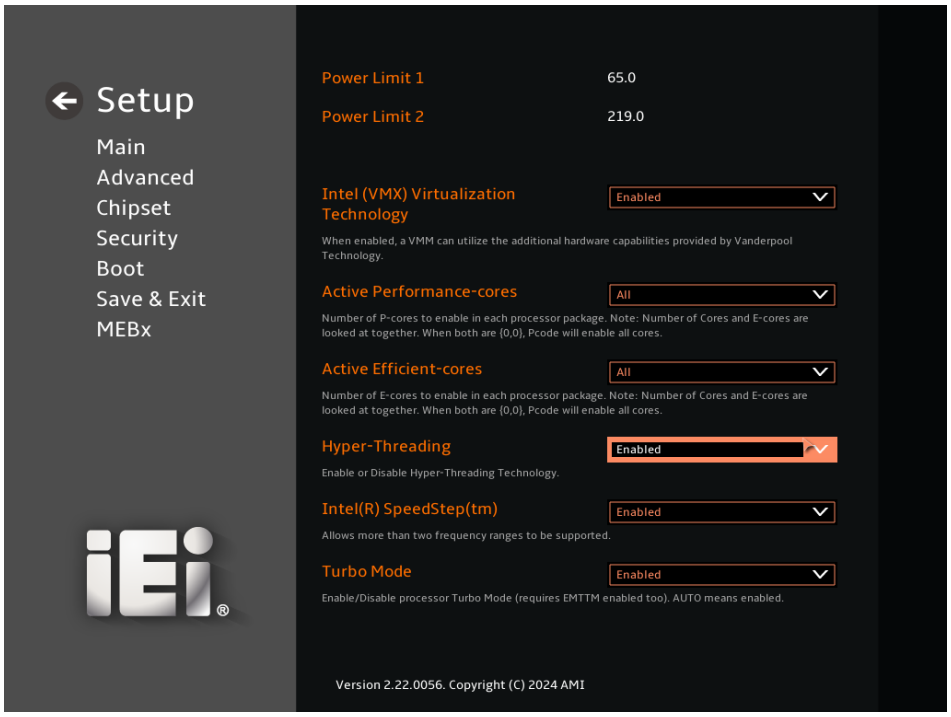
BIOS Menu 5: Advanced (2/2)

5.3.1 CPU Configuration

Use the **CPU Configuration** menu (**BIOS Menu 6**) to view detailed CPU specifications or enable the Intel Virtualization Technology.



BIOS Menu 6: CPU Configuration (1/3)



BIOS Menu 7: CPU Configuration (2/3)

BIOS Menu 8: CPU Configuration (3/3)

➔ **Intel (VMX) Virtualization Technology [Enabled]**

Use the **Intel (VMX) Virtualization Technology** option to enable or disable virtualization on the system. When combined with third party software, Intel® Virtualization technology allows several OSs to run on the same system at the same time.

➔	**Disabled**		Disables Intel Virtualization Technology.
➔	**Enabled**	**DEFAULT**	Enables Intel Virtualization Technology.

➔ **Active Performance Cores [All]**

Use the **Active Performance Cores** BIOS option to enable numbers of P-cores in the processor package.

➔	**All**	**DEFAULT**	Enable all P-cores in the processor package.
➔	**1**		Enable one P-core in the processor package.

➔ **Active Efficient Cores [All]**

Use the **Active Efficient Cores** BIOS option to enable numbers of E-cores in the processor package.

➔	**All**	**DEFAULT**	Enable all E-cores in the processor package.
➔	**0**		Enable zero E-core in the processor package.
➔	**1**		Enable one E-cores in the processor package.
➔	**2**		Enable two E-cores in the processor package.
➔	**3**		Enable three E-cores in the processor package.
➔	**4**		Enable four E-cores in the processor package.
➔	**5**		Enable five E-cores in the processor package.
➔	**6**		Enable six E-cores in the processor package.
➔	**7**		Enable seven E-cores in the processor package.

➔ **Hyper-Threading [Enabled]**

Use the **Hyper-Threading** option to enable or disable the **Hyper-Threading** Technology.

➔ **Disabled**		Disables Hyper-Threading Technology
➔ **Enabled**	**DEFAULT**	Enables Hyper-Threading Technology

➔ **Intel(R) SpeedStep(tm) [Enabled]**

Use the **Intel(R) SpeedStep(tm)** option to enable or disable the Intel® SpeedStep Technology which allows more than two frequency ranges to be supported.

➔ **Disabled**		Disables Intel® SpeedStep Technology
➔ **Enabled**	**DEFAULT**	Enables Intel® SpeedStep Technology

➔ **Turbo Mode [Enabled]**

Use the **Turbo Mode** option to enable or disable Turbo Mode which requires Intel Speed Step or Intel Speed Shift to be available and enabled.

➔ **Disabled**		Disables Turbo Mode Technology
➔ **Enabled**	**DEFAULT**	Enables Turbo Mode Technology

➔ **C states [Disabled]**

Use the **C states** option to enable or disable CPU power management which allows CPU to go to C states when it is not 100% utilized.

➔ **Disabled**	**DEFAULT**	Disables CPU power management
➔ **Enabled**		Enables CPU power management

➔ **Power Limit 1 [0]**

Use the + or – key to change the **Power Limit 1** value. BIOS will program the default values for Limit 1 and Power Limit 1 Time Window. For 12.50W, enter 12500.

➔ **Power Limit 1 Time Window [0]**

Use the **Power Limit 1 Time Window** option to select the PL1 time duration. The value may vary from 0 to 128. For 0 is the default value

➔ **Power Limit 2 [0]**

Use the + or – key to change the **Power Limit 2** value. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500.

5.3.1.1 Efficient-core Information

Use the **Efficient-core Information** menu (**BIOS Menu 11**) to display the E-core information.

BIOS Menu 9: Efficient-core Information

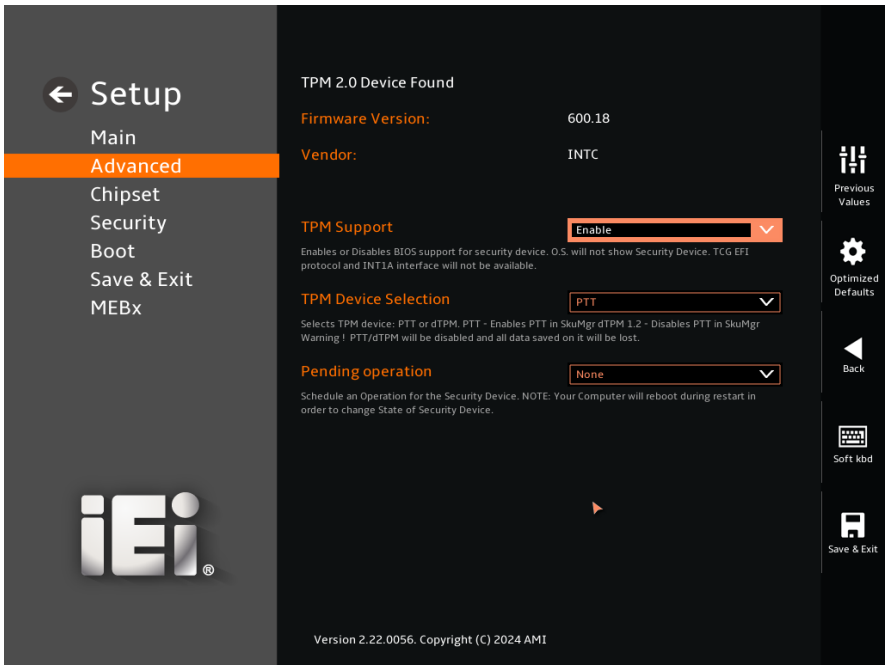
5.3.1.2 Performance-core Information

Use the **Performance-core Information** menu (**BIOS Menu 11**) to display the P-core information.

BIOS Menu 10: Performance-core Information

5.3.2 Trusted Computing

Use the **Trusted Computing** menu (**BIOS Menu 11**) to configure settings related to the Trusted Computing Group (TCG) Trusted Platform Module (TPM).



BIOS Menu 11: PCH-FW Configuration

➔ **TPM Support [Enable]**

Use the **TPM Support** option to select TPM device.

➔ **Disable** TPM support is disabled.

➔ **Enable** **DEFAULT** TPM support is enabled.

➔ **TPM Device Selection [PTT]**

Use the **TPM Device Selection** option to enable or disable BIOS support for security device.

➔ **dTPM.PTT** dTPM.PTT support is enabled.

➔ **PTT** **DEFAULT** PTT support is enabled.

➔ **Pending Operation [None]**

Use the **Pending Operation** option to schedule an operation for the security device.

➔ **None**	**DEFAULT**	TPM information is previous.S
➔ **TPM Clear**		TPM information is cleared

5.3.3 iEi One Key Recovery 2

The **iEi One Key Recovery 2** menu (**BIOS Menu 12**) configures iEi One Key Recovery 2.

BIOS Menu 12: iEi One Key Recovery 2 Settings

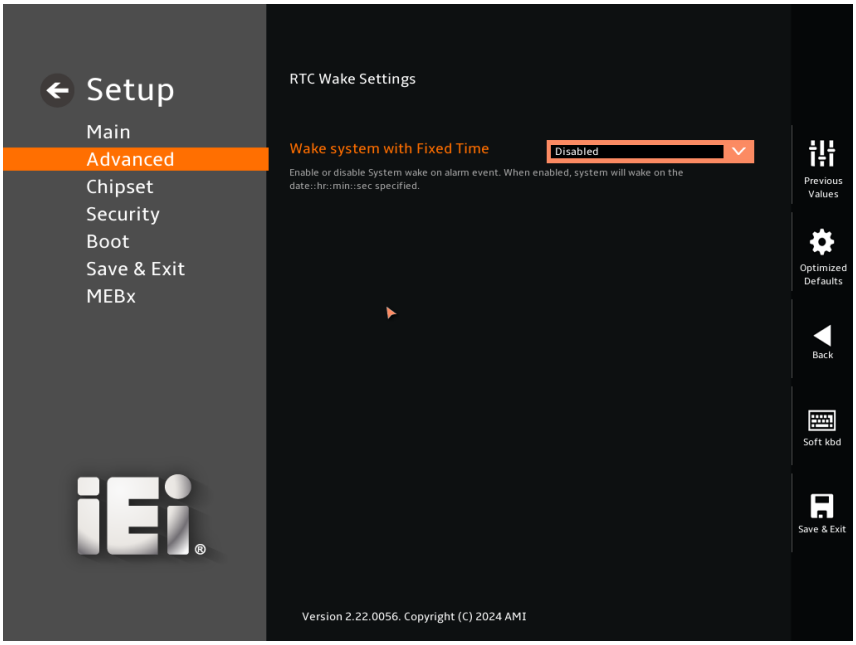
➔ **Auto Recovery Function [Disabled]**

Use the **Auto Recovery Function** option to enable or disable watchdog function, when OS crashes, it will automatically recover system.

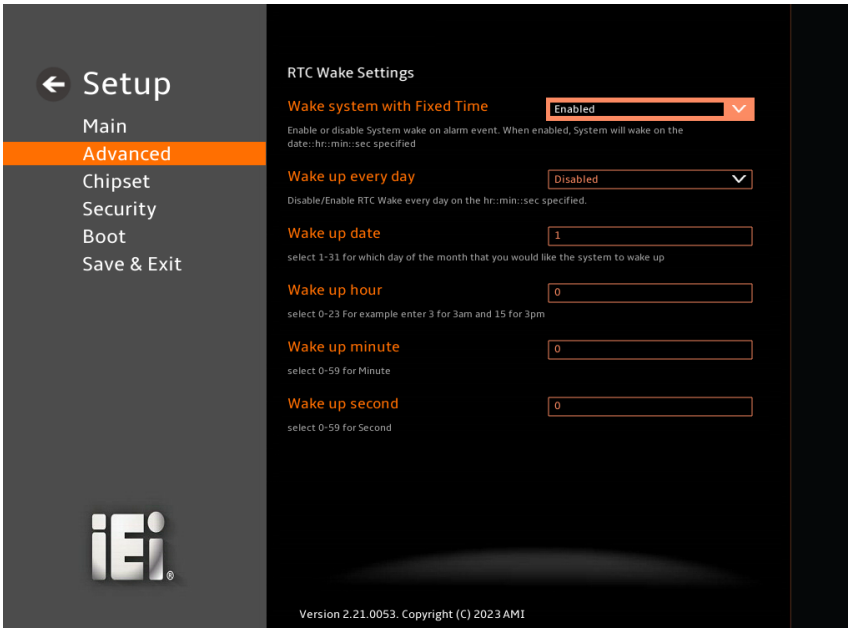
➔ **Disable**		TPM support is disabled.
➔ **Enable**	**DEFAULT**	TPM support is enabled.

5.3.4 RTC Wake Settings

The **RTC Wake Settings** menu (**BIOS Menu 13**) configures RTC wake event.



BIOS Menu 13: RTC Wake Settings (1/2)



BIOS Menu 14: RTC Wake Settings (2/2)

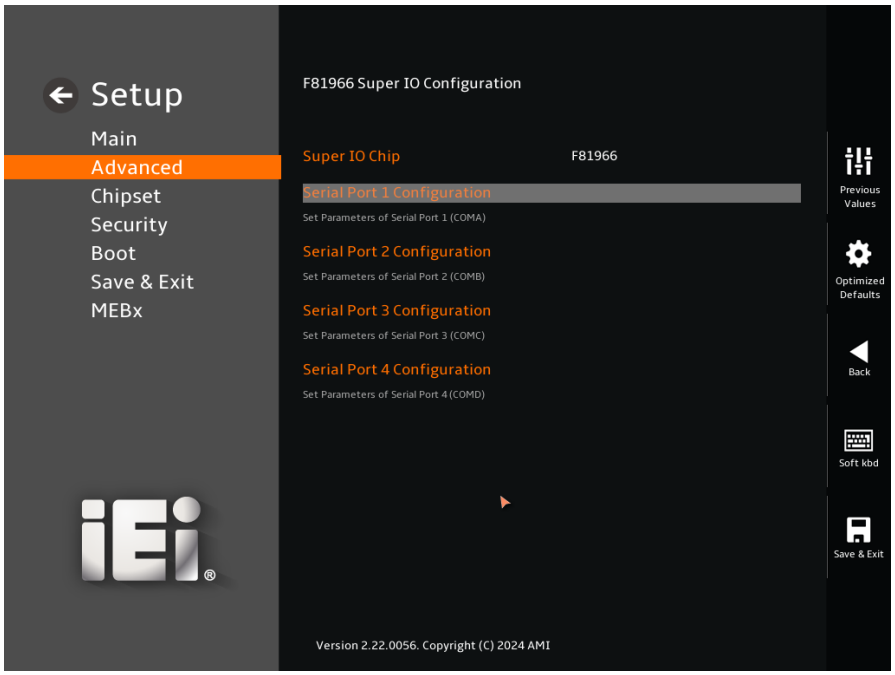
➔ **Wake system with Fixed Time [Enabled]**

Use the **Wake system with Fixed Time** option to enable or disable the system wake on alarm event.

➔ **Disabled**		The real time clock (RTC) cannot generate a wake event
➔ **Enabled**	**DEFAULT**	If selected, the **Wake up every day** option appears allowing you to enable to disable the system to wake every day at the specified time. Besides, the following options appear with values that can be selected: Wake up date Wake up hour Wake up minute Wake up second After setting the alarm, the computer turns itself on from a suspend state when the alarm goes off.

5.3.5 F81966 Super IO Configuration

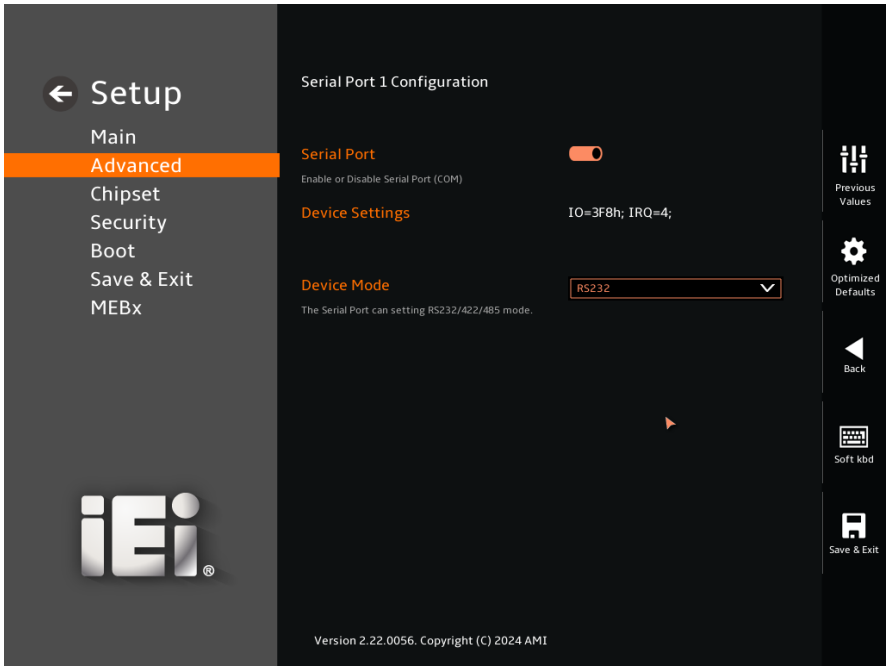
Use the **F81966 Super IO Configuration** menu (**BIOS Menu 15**) to set or change the configurations for serial ports.



BIOS Menu 15: F81966 Super IO Configuration

5.3.5.1 Serial Port 1 Configuration

Use the **Serial Port 1 Configuration** menu (**BIOS Menu 16**) to configure the serial port n.



BIOS Menu 16: Serial Port 1 Configuration Menu

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**		Disable the serial port
➔ **Enabled**	**DEFAULT**	Enable the serial port

➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.

➔ **IO=3F8h; IRQ=4**	Serial Port I/O port address is 3F8h and the interrupt address is IRQ4

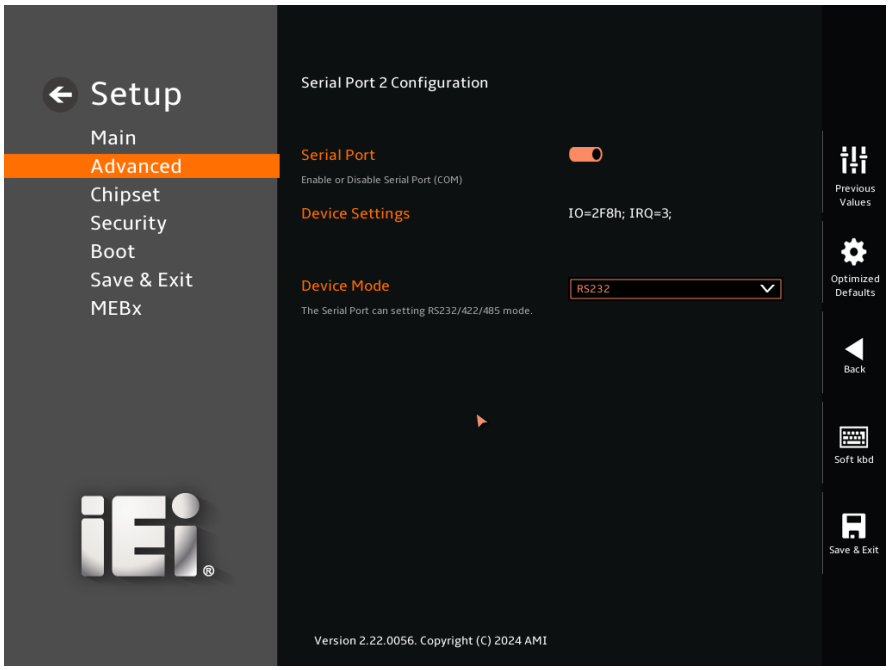
➔ **Device Mode [RS232]**

Use the **Device Mode** option to change the serial port mode.

➔ **RS232**	**DEFAULT**	The serial port mode is RS-232
RS422 with Register		The serial port mode is RS-422
RS485 with Register		The serial port mode is RS-485

5.3.5.2 Serial Port 2 Configuration

Use the **Serial Port 2 Configuration** menu (**BIOS Menu 17**) to configure the serial port n.



BIOS Menu 17: Serial Port 2 Configuration Menu

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**		Disable the serial port
➔ **Enabled**	**DEFAULT**	Enable the serial port

➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.

➔ **IO=2F8h; IRQ=3**		Serial Port I/O port address is 2F8h and the interrupt address is IRQ3

➔ **Device Mode [RS232]**

Use the **Device Mode** option to change the serial port mode.

➔ **RS232**	**DEFAULT**	The serial port mode is RS-232
RS422 with Register		The serial port mode is RS-422
RS485 with Register		The serial port mode is RS-485

5.3.5.3 Serial Port 3 Configuration

Use the **Serial Port 3 Configuration** menu (**BIOS Menu 18**) to configure the serial port 3.

BIOS Menu 18: Serial Port 3 Configuration Menu

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**	Disable the serial port

➔ **Enabled** **DEFAULT** Enable the serial port

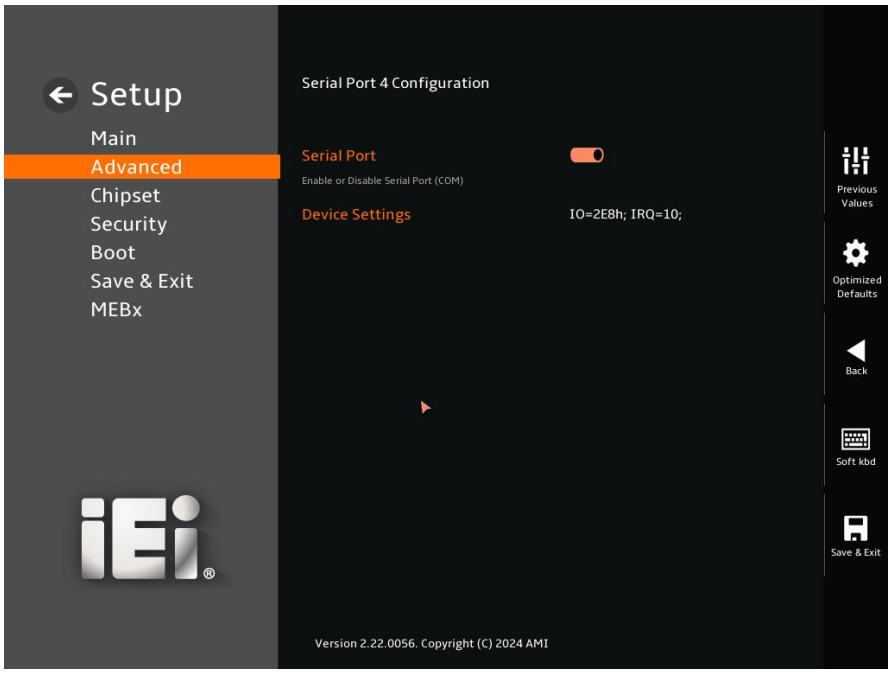
➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.

➔ **IO=2E0h; IRQ=10** Serial Port I/O port address is 2E0h and the interrupt address is IRQ10

5.3.5.4 Serial Port 4 Configuration

Use the **Serial Port 4 Configuration** menu (**BIOS Menu 19**) to configure the serial port 4.



BIOS Menu 19: Serial Port 4 Configuration Menu

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled** Disable the serial port

➔ **Enabled** **DEFAULT** Enable the serial port

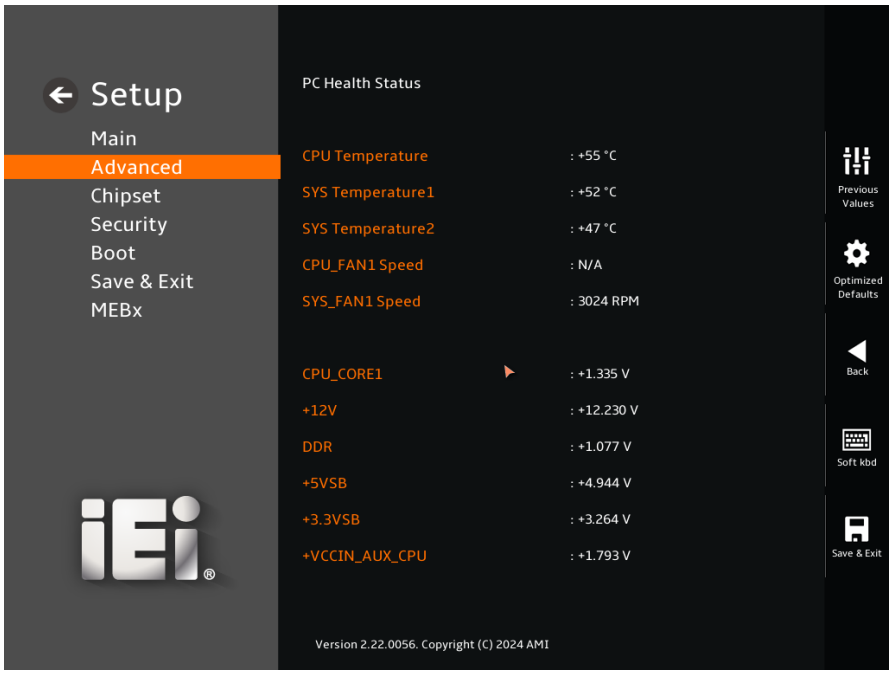
➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.

➔ **IO=2E8h; IRQ=10**	Serial Port I/O port address is 2E8h and the interrupt address is IRQ10

5.3.6 EC KB9068 H/W Monitor

The **EC KB9068 H/W Monitor** menu (**BIOS Menu 20**) contains the smart fan mode configuration submenu and shows the state of H/W real-time operating temperature, fan speeds and system voltages.



BIOS Menu 20: EC KB9068 H/W Monitor (1/2)

BIOS Menu 21: EC KB9068 H/W Monitor (2/2)

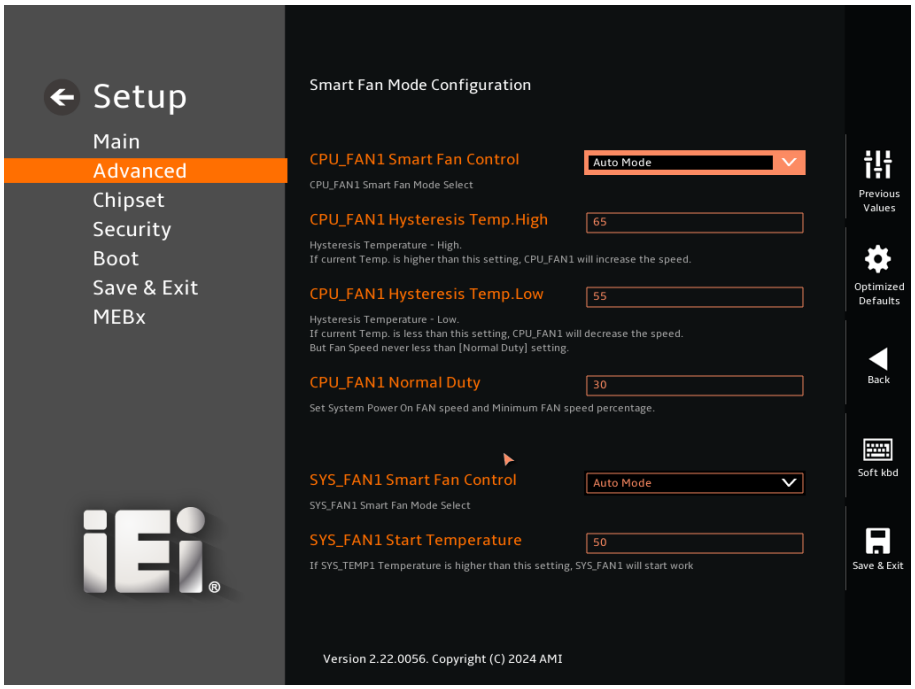
➔ PC Health Status

The following system parameters and values are shown. The system parameters that are monitored are:

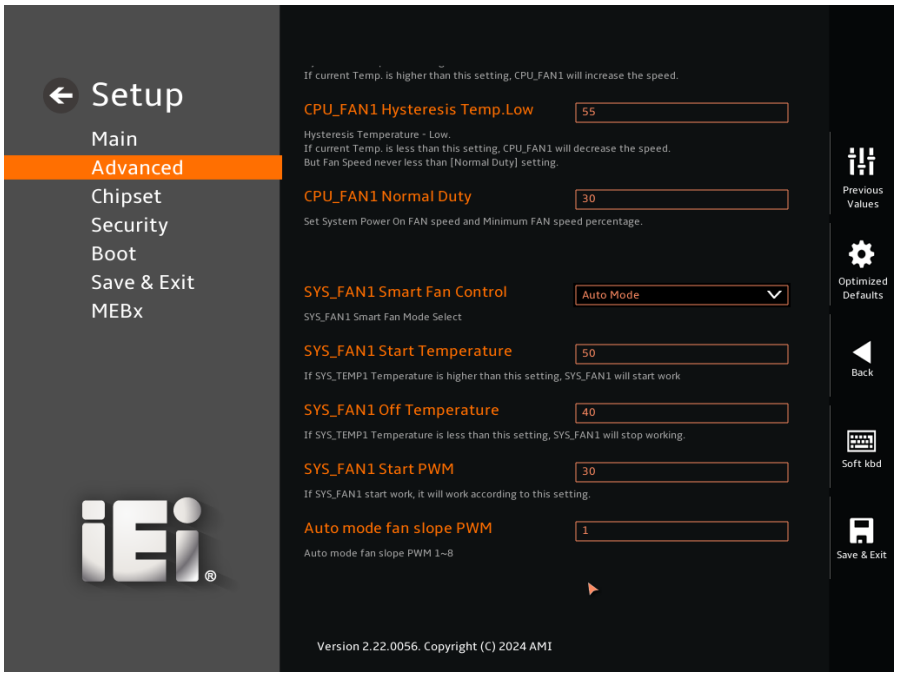
- System Temperatures:
  - CPU Temperature
  - System Temperature1
  - System Temperature2
- Fan Speeds:
  - CPU_Fan1 Speed
  - SYS_Fan1 Speed
- Voltages:
  - VCCCORE
  - +5VS
  - 12S
  - DDR
  - +DC_IN

5.3.6.1 Smart Fan Mode Configuration

Use the **Smart Fan Mode Configuration** submenu (**BIOS Menu 22**) to configure the CPU/system fan start/off temperature and control mode.



BIOS Menu 22: Smart Fan Mode Configuration (1/2)



BIOS Menu 23: Smart Fan Mode Configuration (2/2)

➔ **CPU_FAN1 Smart Fan Control [Auto Mode]**

Use the **CPU_FAN1 Smart Fan Control** option to configure the CPU Smart Fan.

➔ **Manual Mode**		The fan spins at the speed set in Manual Mode settings.
➔ **Auto Mode**	**DEFAULT**	The fan adjusts its speed using Auto Mode settings.

➔ **CPU_FAN1 Hysteresis Temp.High [65]**

If the current CPU temperature is higher than this setting, CPU_FAN1 will increase the speed.

➔ **CPU_FAN1 Hysteresis Temp.Low [55]**

If the current CPU temperature is lower than this setting, CPU_FAN1 will decrease the speed. But fan speed never less than [Normal Duty] setting.

➔ **CPU_FAN1 Normal Duty [30]**

Use the **CPU_FAN1 Start PWM** option to set the system power on fan speed and minimum fan speed percentage. Use the + or – key to change the value or enter a decimal number .

➔ **SYS_FAN1 Smart Fan Control [Auto Mode]**

Use the **Smart Fan Control** option to configure the System Smart Fan.

➔ **Manual Mode**		The fan spins at the speed set in Manual Mode settings.
➔ **Auto Mode**	**DEFAULT**	The fan adjusts its speed using Auto Mode settings.

➔ **SYS_FAN1 Start Temperature [50]**

If the System temperature is between **fan off** and **fan start**, the fan speed change to **fan start PWM**. To set a value, Use the + or – key to change the value or enter a decimal number between 1 and 100.

➔ **SYS_FAN1 Off Temperature [40]**

If the System temperature is lower than the value set this option, the fan speed change to be lowest. To set a value, Use the + or – key to change the value or enter a decimal number between 1 and 100.

➔ **SYS_FAN1 Start PWM [30]**

Use the **SYS_FAN1 Start PWM** option to set the PWM start value. Use the + or – key to change the value or enter a decimal number between 1 and 100.

➔ **CPU_FAN1 Off Temperature**

If the CPU temperature is lower than the value set this option, the fan speed change to be lowest. To set a value, Use the + or – key to change the value or enter a decimal number between 1 and 100.

➔ **CPU_FAN1 Start PWM**

Use the **CPU_FAN1 Start PWM** option to set the PWM start value. Use the + or – key to change the value or enter a decimal number between 1 and 100.

5.3.7 Serial Port Console Redirection

The **Serial Port Console Redirection** menu (**BIOS Menu 24 & BIOS Menu 25**) allows the console redirection options to be configured. Console Redirection allows users to maintain a system remotely by re-directing keyboard input and text output through the serial port.

BIOS Menu 24: Serial Port Console Redirection (1/3)

BIOS Menu 25: Serial Port Console Redirection (2/3)

BIOS Menu 26: Serial Port Console Redirection (3/3)

➔ **Console Redirection [Disabled]**

Use **Console Redirection** option to enable or disable the console redirection function.

➔ **Disabled** **DEFAULT** Disabled the console redirection function

➔ **Enabled** Enabled the console redirection function

The **Console Redirection Settings** submenu will be available when the **Console Redirection** option is enabled.

5.3.7.1 Console Redirection Settings

The following options are available in the **Console Redirection Settings** submenu (**BIOS Menu 27**) when the **COM Console Redirection** (for COM1 to COM6) option is enabled.

BIOS Menu 27: COM Console Redirection Settings

➔ **Terminal Type [ANSI]**

Use the **Terminal Type** option to specify the remote terminal type.

➔ **VT100** The target terminal type is VT100

➔ **VT100+** The target terminal type is VT100+

➔ **VT-UTF8** The target terminal type is VT-UTF8

➔	**ANSI**	**DEFAULT**	The target terminal type is ANSI

➔ **Bits per second [115200]**

Use the **Bits per second** option to specify the serial port transmission speed. The speed must match on the other side. Long or noisy lines may require lower speeds.

➔	**9600**		Sets the serial port transmission speed at 9600.
➔	**19200**		Sets the serial port transmission speed at 19200.
➔	**38400**		Sets the serial port transmission speed at 38400.
➔	**57600**		Sets the serial port transmission speed at 57600.
➔	**115200**	**DEFAULT**	Sets the serial port transmission speed at 115200.

➔ **Data Bits [8]**

Use the **Data Bits** option to specify the number of data bits.

➔	**7**		Sets the data bits at 7.
➔	**8**	**DEFAULT**	Sets the data bits at 8.

➔ **Parity [None]**

Use the **Parity** option to specify the parity bit that can be sent with the data bits for detecting the transmission errors.

➔	**None**	**DEFAULT**	No parity bit is sent with the data bits.
➔	**Even**		The parity bit is 0 if the number of ones in the data bits is even.
➔	**Odd**		The parity bit is 0 if the number of ones in the data bits is odd.
➔	**Mark**		The parity bit is always 1. This option does not allow for error detection.
➔	**Space**		The parity bit is always 0. T This option does not allow for error detection.

➔ **Stop Bits [1]**

Use the **Stop Bits** option to specify the number of stop bits used to indicate the end of a serial data packet. Communication with slow devices may require more than 1 stop bit.

➔	**1**	**DEFAULT**	Sets the number of stop bits at 1.
➔	**2**		Sets the number of stop bits at 2.

5.3.8 NVMe Configuration

Use the **NVMe Configuration** (**BIOS Menu 28**) menu to display the NVMe controller and device information.

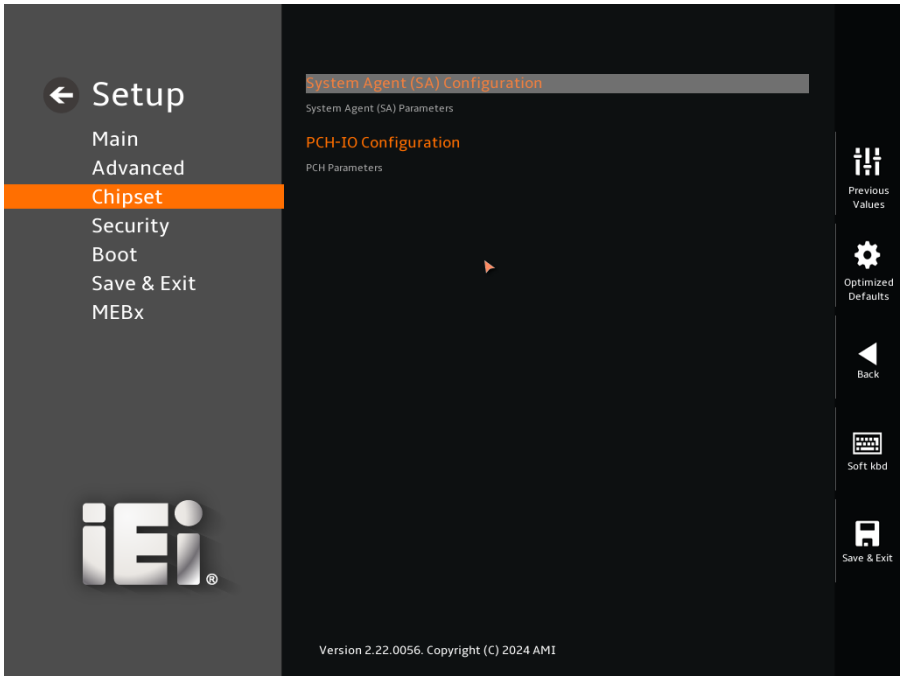
BIOS Menu 28: NVMe Configuration

5.4 Chipset

Use the **Chipset** menu (**BIOS Menu 29**) to access the PCH IO and System Agent (SA) configuration menus.

WARNING!

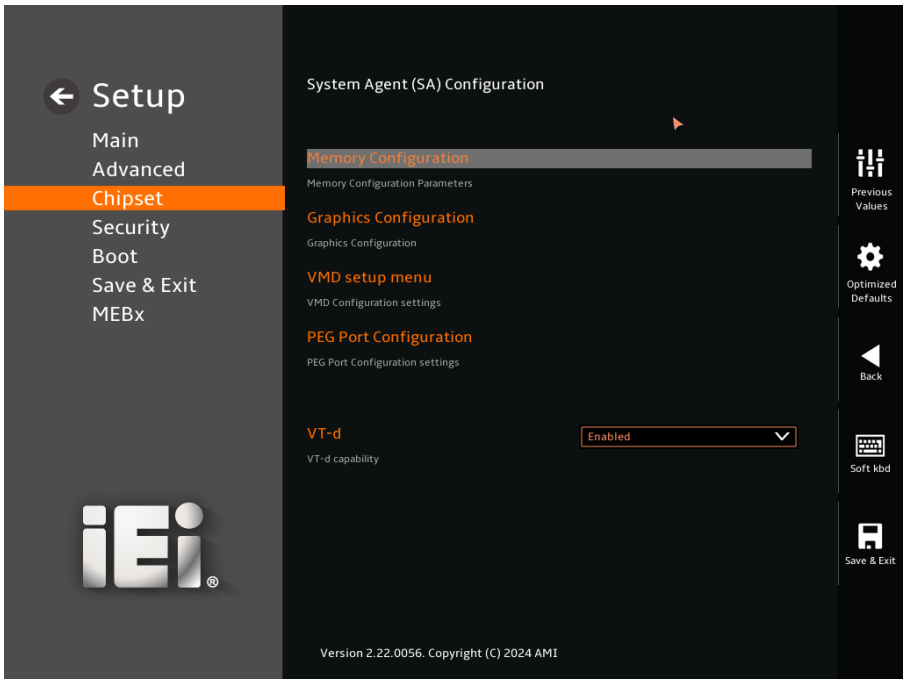
Setting the wrong values for the Chipset BIOS selections in the Chipset BIOS menu may cause the system to malfunction.



BIOS Menu 29: Chipset

5.4.1 System Agent (SA) Configuration

Use the **System Agent (SA) Configuration** menu (**BIOS Menu 30**) to configure the System Agent (SA) parameters.



BIOS Menu 30: System Agent (SA) Configuration

➔ **VT-d [Enabled]**

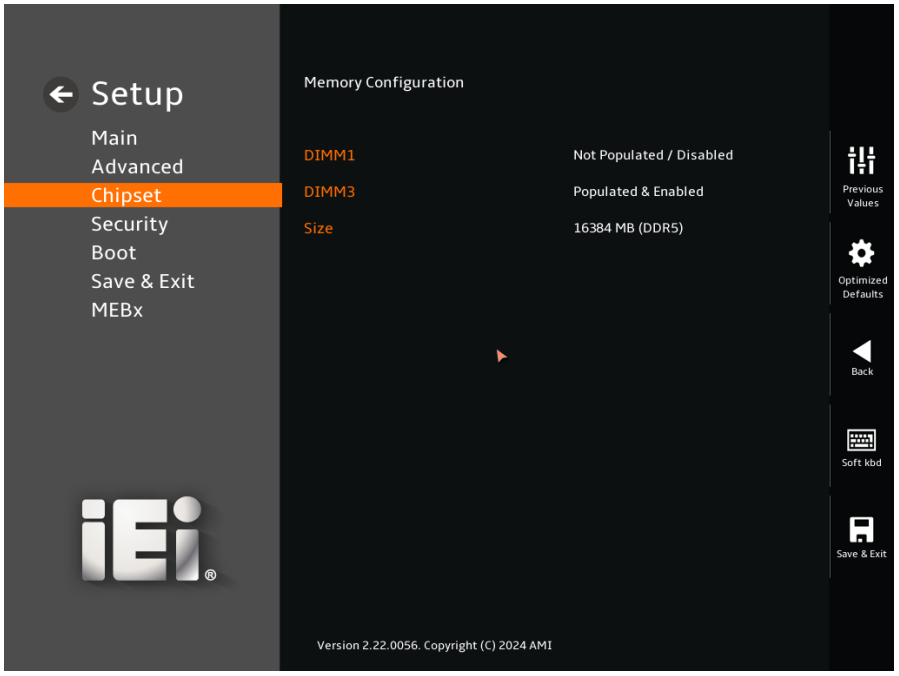
Use the **VT-d** option to enable or disable the VT-d capability.

➔ **Disabled** Disable the VT-d capability

➔ **Enabled** **DEFAULT** Enable the VT-d capability

5.4.1.1 Memory Configuration

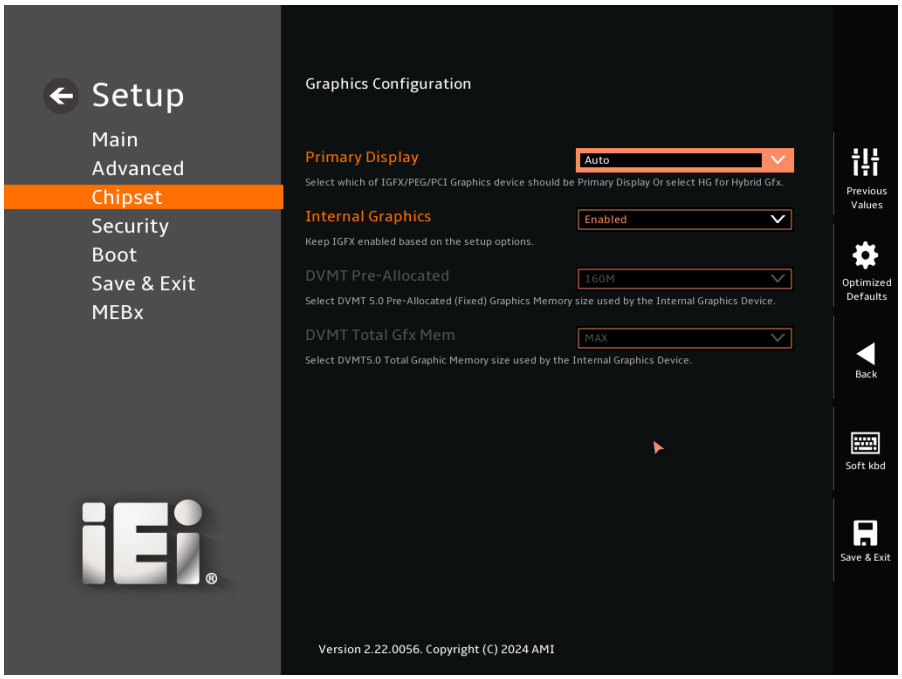
Use the **Memory Configuration** submenu (**BIOS Menu 31**) to view memory information.



BIOS Menu 31: Memory Configuration

5.4.1.2 Graphics Configuration

Use the **Graphics Configuration** (**BIOS Menu 32**) menu to configure the video device connected to the system.



BIOS Menu 32: Graphics Configuration

➔ **Primary Display [Auto]**

Use the **Primary Display** option to select the primary graphics controller the system uses. The following options are available:

- Auto **Default**
- IGFX
- PEG
- PCI
- HG

➔ **Internal Graphics [Enabled]**

Use the **Internal Graphics** option to configure whether to keep IGFX enabled. If user wants to support dual display by internal graphics and external graphics, this Internal Graphics

option should be set to Enabled and the above Primary Display option should be set to IGFX.

➔	**Auto**		Auto mode
➔	**Disabled**		Disables IGFX.
➔	**Enabled**	**Default**	Enables IGFX.

➔ **DVMT Pre-Allocated [160M]**

Use the **DVMT Pre-Allocated** option to set the amount of system memory allocated to the integrated graphics processor when the system boots. The system memory allocated can then only be used as graphics memory, and is no longer available to applications or the operating system. Configuration options are listed below:

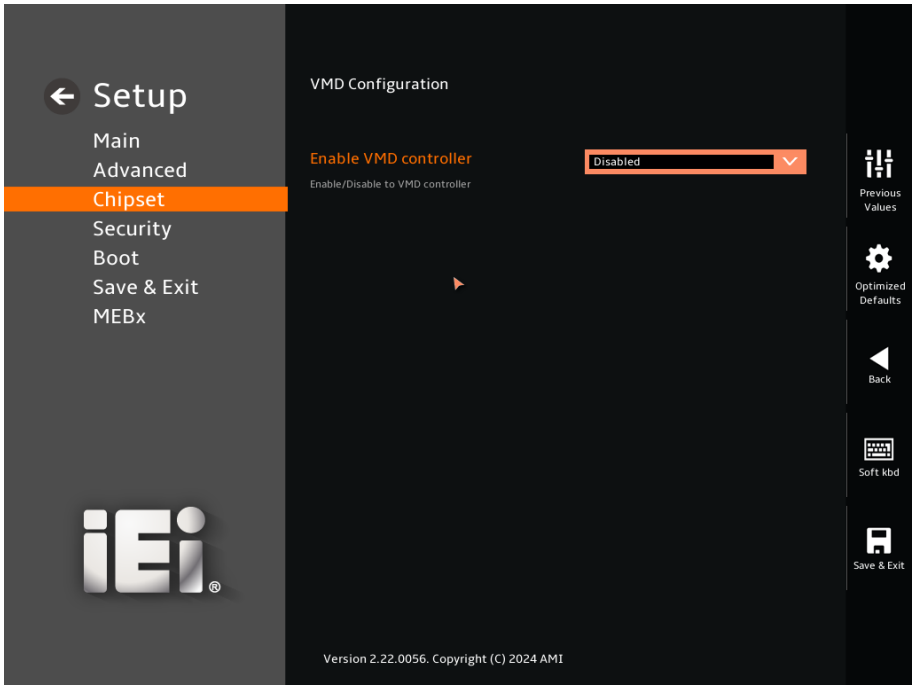
- 80M
- 160M **Default**

➔ **DVMT Total Gfx Mem [MAX]**

Use the **DVMT Total Gfx Mem** option to select DVMT5.0 total graphic memory size used by the internal graphic device. The following options are available:

- 128M
- 256M
- MAX **Default**

5.4.1.3 VMD Configuration



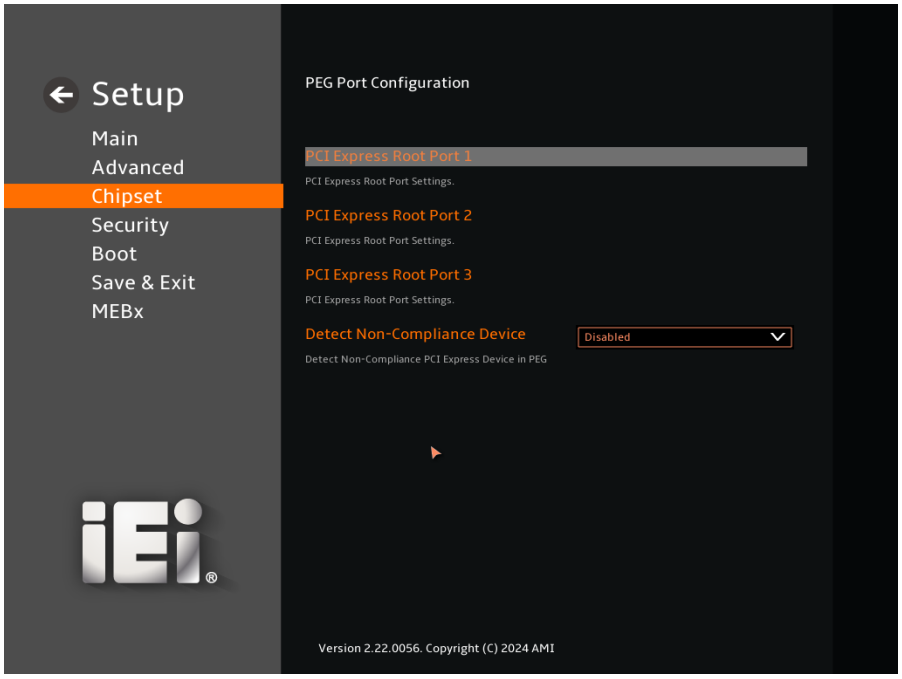
BIOS Menu 33: VMD Configuration

➔ **Enable VMD controller [Disabled]**

Use the **Enable VMD controller** option to enable or disable VMD controller.

➔ **Disabled**	**Default**	Disable VMD controller.
➔ **Enabled**		Enable VMD controller.

5.4.1.4 PEG Port Configuration



BIOS Menu 34: PEG Port Configuration

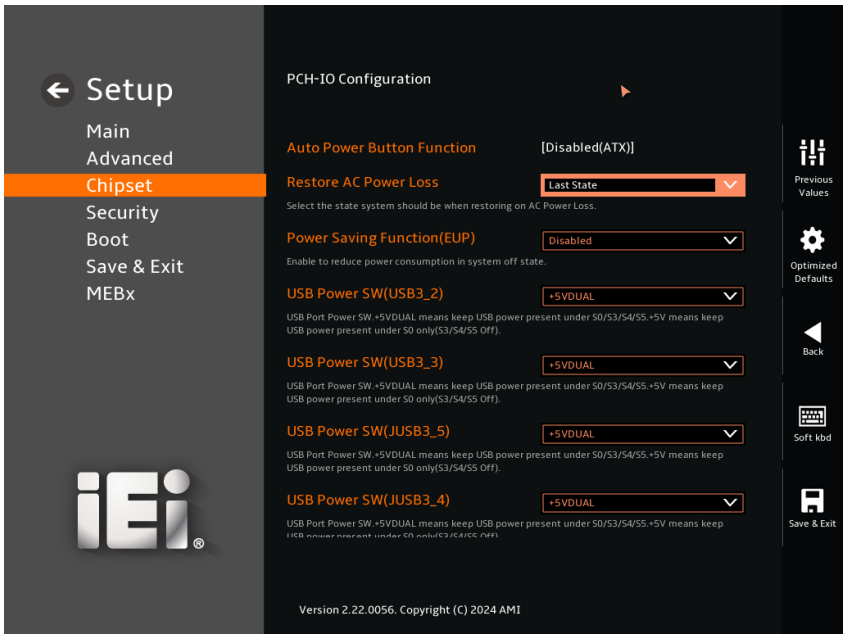
➔ **Detect Non-Compliance Device [Disabled]**

Use the **Detect Non-Compliance Device** option to detect non-compliance PCIe device in PEG.

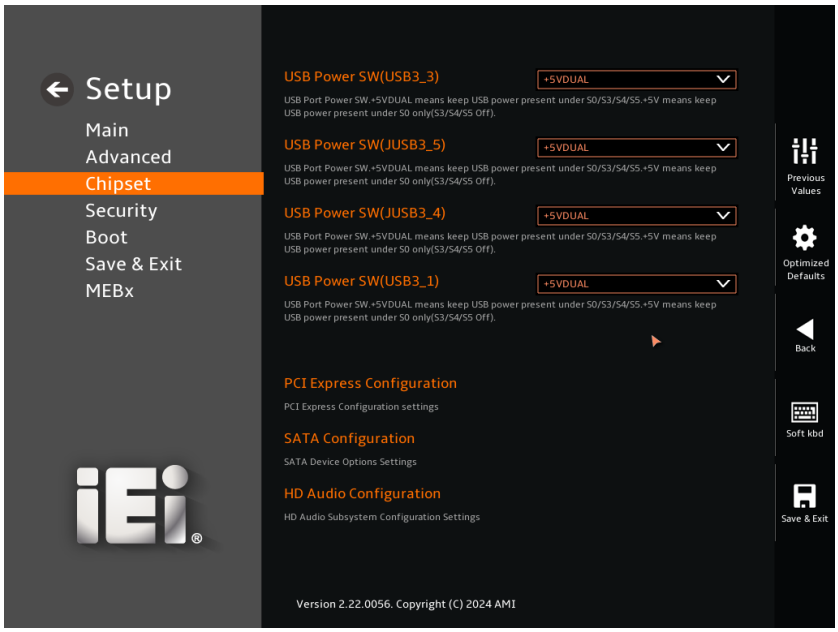
➔	**Disabled**	**DEFAULT**	Do not detect non-compliance PCIe device in PEG
➔	**Enabled**		Detect non-compliance PCIe device in PEG

5.4.2 PCH-IO Configuration

Use the **PCH-IO Configuration** menu (**BIOS Menu 35**) to configure the PCH parameters.



BIOS Menu 35: PCH-IO Configuration (1/2)



BIOS Menu 36: PCH-IO Configuration (2/2)

➔ **Auto Power Button Function [Disabled (ATX)]**

Use the **Auto Power Button Function** BIOS option to show the power mode state. Use the **J_ATX_AT1** to switch the AT/ATX power mode.

➔ **Enabled (AT)**		The system power mode is AT.
➔ **Disabled (ATX)**		The system power mode is ATX.

➔ **Restore AC Power Loss [Last State]**

Use the **Restore AC Power Loss** BIOS option to specify what state the system returns to if there is a sudden loss of power to the system when the power mode is ATX.

➔ **Power Off**		The system remains turned off
➔ **Power On**		The system turns on
➔ **Last State**	**DEFAULT**	The system returns to its previous state. If it was on, it turns itself on. If it was off, it remains off.

➔ **Power Saving Function (EUP) [Disabled]**

Use the **Power Saving Function (EUP)** BIOS option to enable or disable the power saving function.

➔ **Disabled**	**DEFAULT**	Power saving function is disabled.
➔ **Enabled**		Power saving function is enabled. It will reduce power consumption when the system is off.

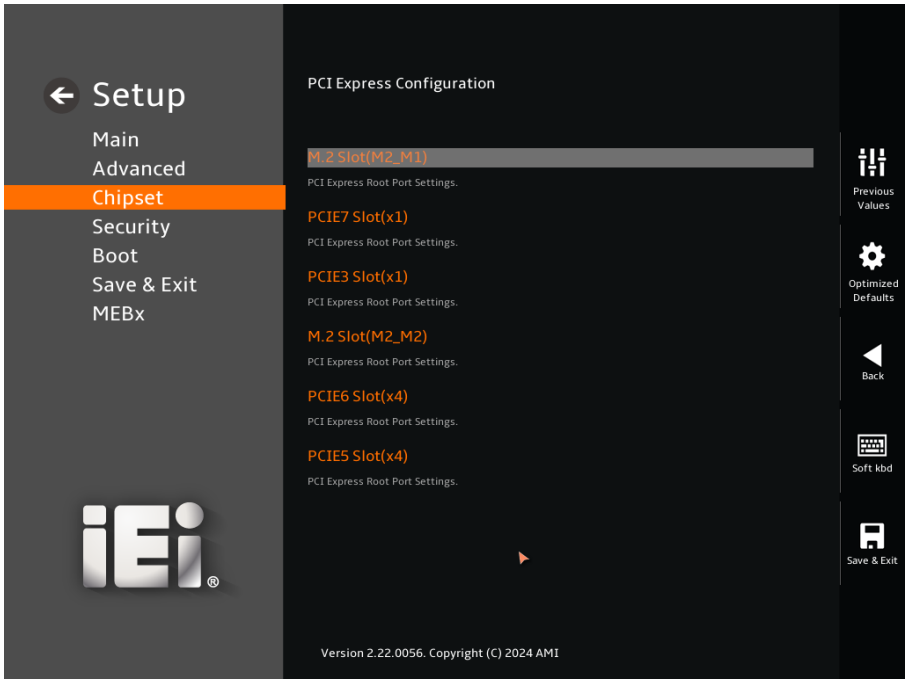
➔ **USB Power state SW [+5VDUAL]**

Use the **USB Power state option** to enable or disable the USB Power.

➔ **+5VDUAL**	**DEFAULT**	USB Power is on.
➔ **+5V**		USB Power is off.

5.4.2.1 PCI Express Configuration

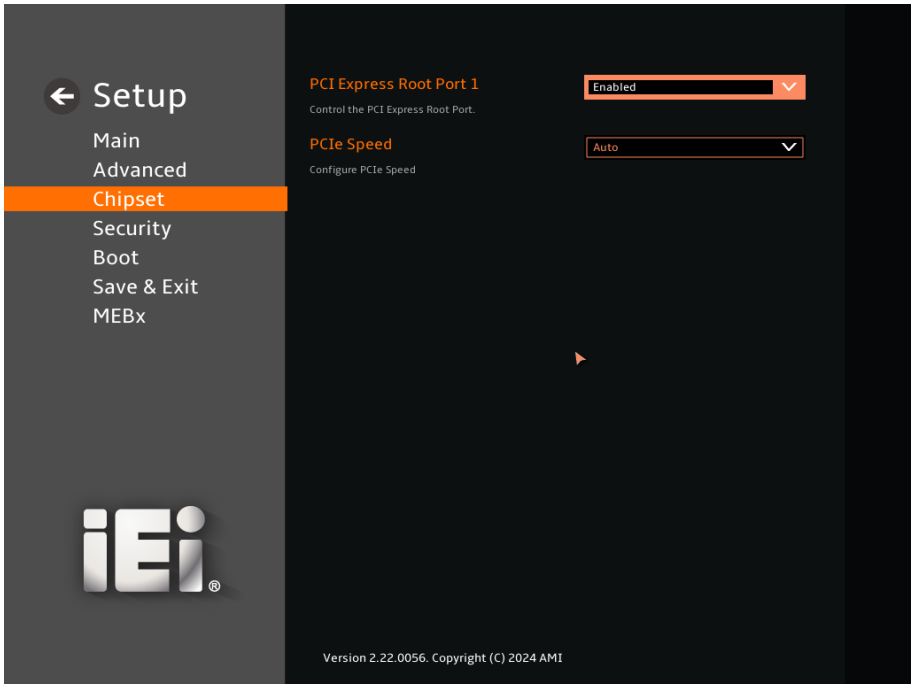
Use the **PCI Express Configuration** submenu (**BIOS Menu 37**) to configure the PCI Express slots.



BIOS Menu 37: PCI Express Configuration

5.4.2.1.1 PCIe Root Port Setting

Use the **M2_M1, PCIE7x1, PCIE3X1, M2_M2, PCIE6X4, PCIE5X4** submenu (**BIOS Menu 38**) to configure the PCI Root Port Setting.



BIOS Menu 38: PCIe Slot Configuration Submenu

➔ **PCIe Speed [Auto]**

Use the **PCIe Speed** option to specify the PCI Express port speed. Configuration options are listed below.

➔ **Auto**	**DEFAULT**	Auto mode.
➔ **Gen1**		Configure PCIe Speed to Gen1.
➔ **Gen2**		Configure PCIe Speed to Gen2.
➔ **Gen3**		Configure PCIe Speed to Gen3.

➔ **Detect Non-Compliance Device [Disabled]**

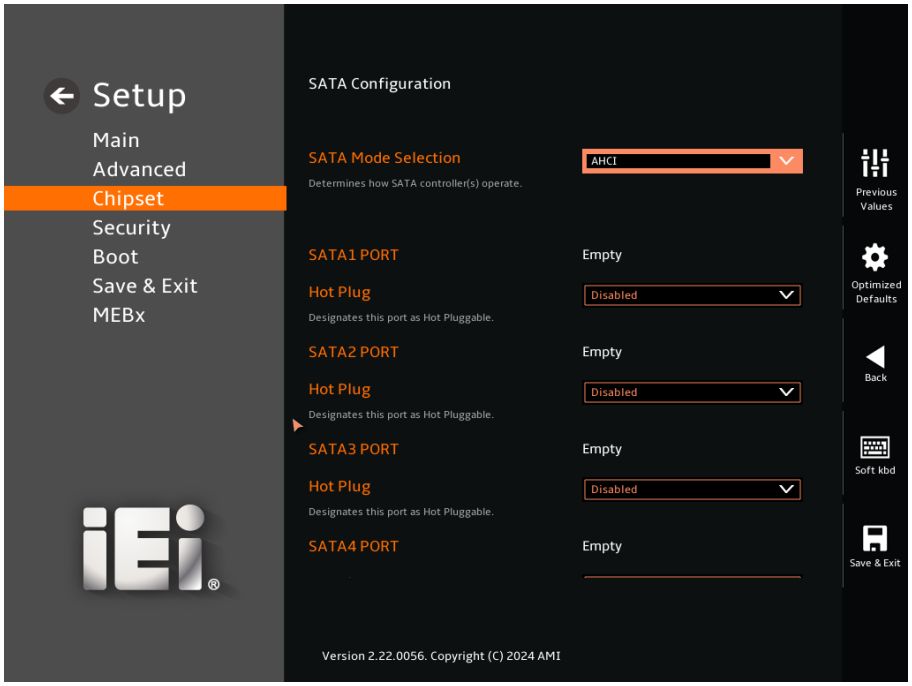
Use the **Detect Non-Compliance Device** option to configure whether to detect if a non-compliance PCI Express device is connected to the PCI Express port.

➔ **Disabled**	**DEFAULT**	Do not detect if a non-compliance PCI Express device is connected to the PCI Express port.

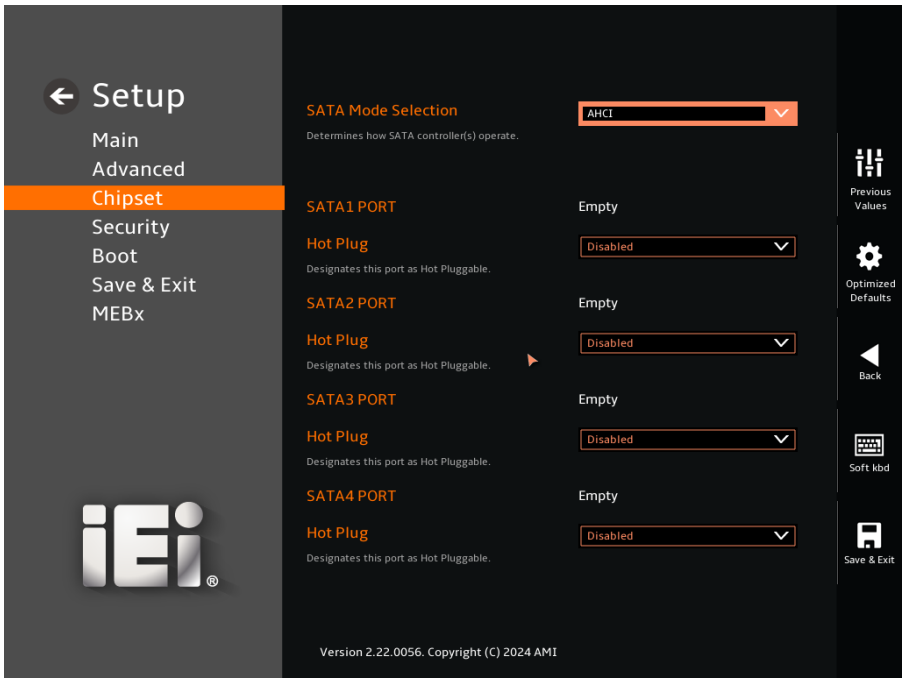
➔ **Enabled** Detect if a non-compliance PCI Express device is connected to the PCI Express port.

5.4.2.2 SATA Configuration

Use the **SATA Configuration** menu (**BIOS Menu 39**) to change and/or set the configuration of the SATA devices installed in the system.



BIOS Menu 39: SATA Configuration (1/2)



BIOS Menu 40: SATA Configuration (2/2)

➔ **SATA Mode Selection [AHCI]**

Use the **SATA Mode Selection** option to determine how the SATA devices operate.

➔ **AHCI**	**DEFAULT**	Configures SATA devices as AHCI device.
➔ **Intel RST Premium With Intel Optane System Acceleration**		Configures SATA devices to the Intel RST Premium With Intel Optane System Acceleration mode.

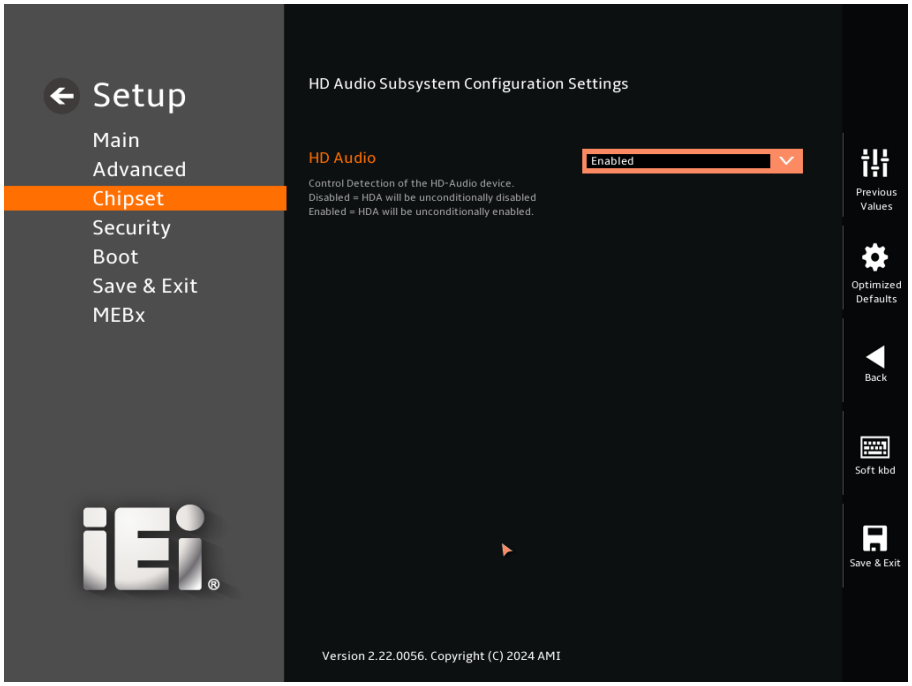
➔ **Hot Plug [Disabled]**

Use the **Hot Plug** option to designate the correspondent port as hot-pluggable.

➔ **Disabled**	**DEFAULT**	Disables the hot-pluggable function of the SATA port.
➔ **Enabled**		Designates the SATA port as hot-pluggable.

5.4.2.3 HD Audio Configuration

Use the **HD Audio Configuration** menu (**BIOS Menu 41**) to configure the PCH Azalia settings.



BIOS Menu 41: HD Audio Configuration

➔ **HD Audio [Enabled]**

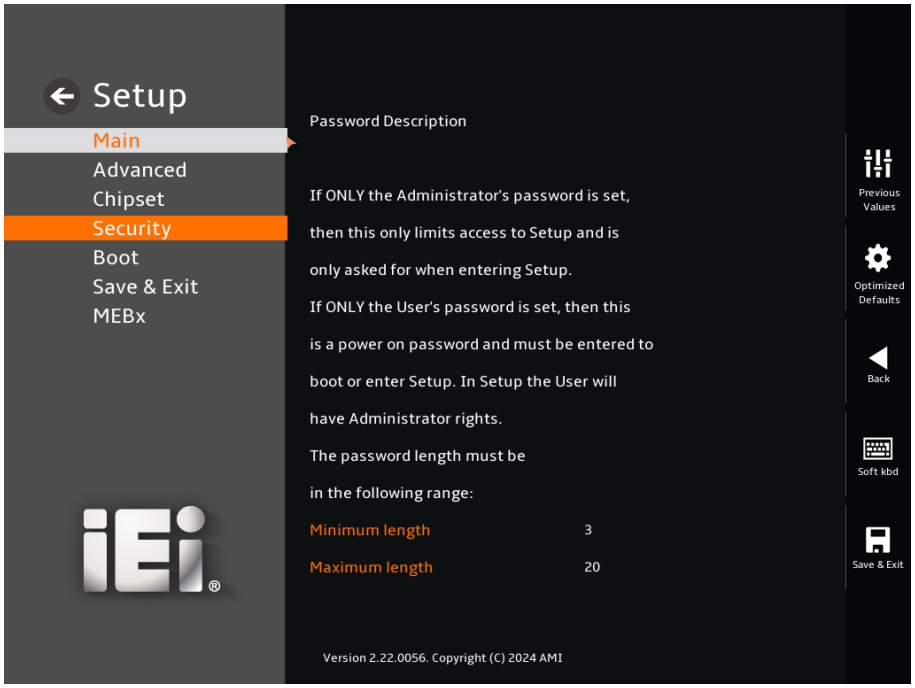
Use the **HD Audio** option to enable or disable the High Definition Audio controller.

➔ **Disabled** The onboard High Definition Audio controller is disabled.

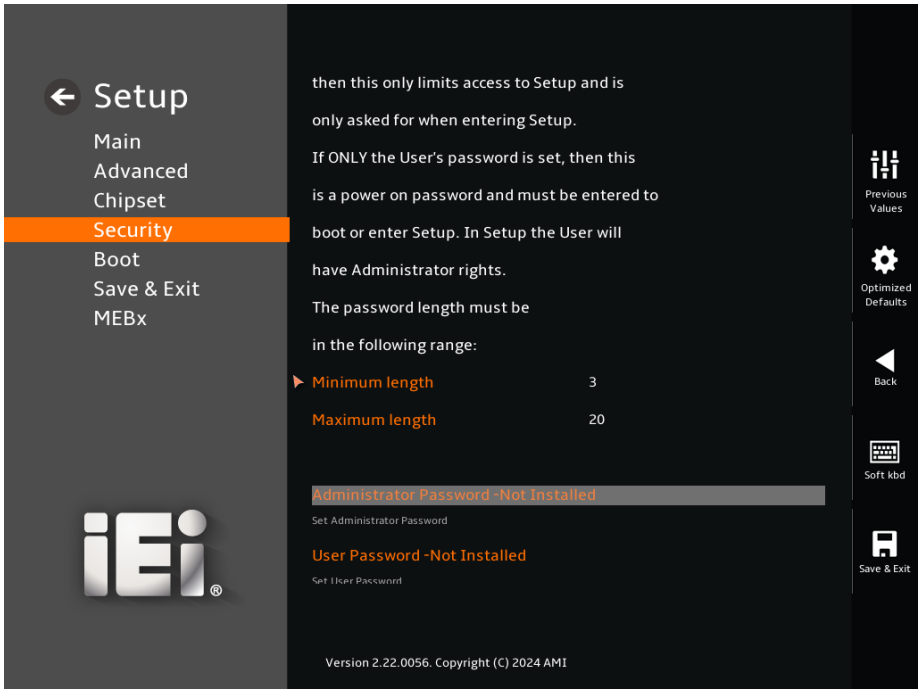
➔ **Enabled** **DEFAULT** The onboard High Definition Audio controller is enabled.

5.5 Security

Use the **Security** menu (**BIOS Menu 43**) to set system and user passwords.



BIOS Menu 42: Security (1/2)



BIOS Menu 43: Security (2/2)

➔ **Administrator Password**

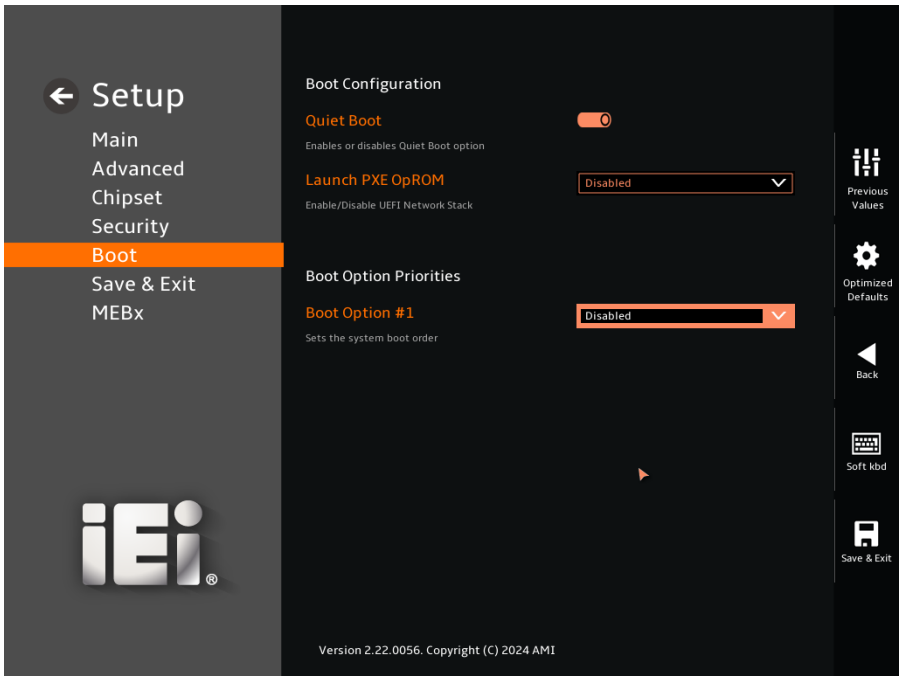
Use the **Administrator Password** to set or change an administrator password.

➔ **User Password**

Use the **User Password** to set or change a user password.

5.6 Boot

Use the **Boot** menu (**BIOS Menu 44**) to configure system boot options.



BIOS Menu 44: Boot

5.6.1 Boot Configuration

➔ **Quiet Boot [Enabled]**

Use the **Quiet Boot** BIOS option to select the screen display when the system boots.

➔ **Disabled** Normal POST messages displayed

➔ **Enabled** **DEFAULT** OEM Logo displayed instead of POST messages

➔ **Launch PXE OpROM [Disabled]**

Use the **Launch PXE OpROM** option to enable or disable boot option for legacy network devices.

➔ **Disabled** **DEFAULT** Ignore all PXE Option ROMs

➔ **Enabled** Load PXE Option ROMs.

5.6.2 Boot Option Priorities

Use the Boot Option # N to choose the system boots from the peripherals you selected. The following Boot Options are listed as an example.

➔ **Boot Option #1**

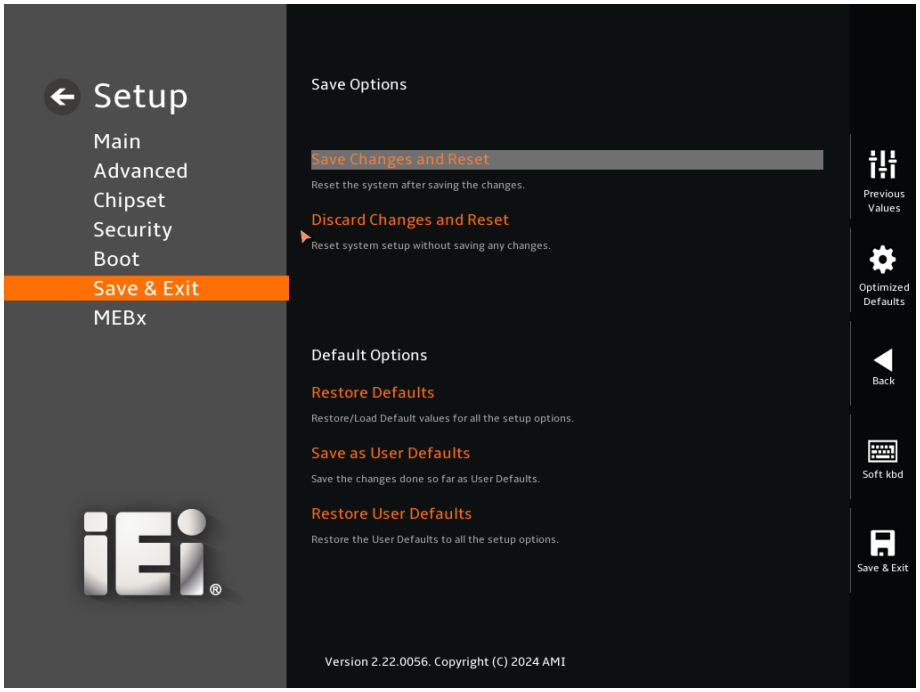
Sets the system boot order **ADATA SP580** as the first priority.

➔ **Windows Boot Manager (P1: ADATA SSD SP580 240GB)**

➔ **Disabled**

5.7 Save & Exit

Use the **Save & Exit** menu (**BIOS Menu 45**) to load default BIOS values, optimal failsafe values and to save configuration changes.



BIOS Menu 45: Save & Exit

➔ **Save Changes and Reset**

Use the **Save Changes and Reset** option to save the changes made to the BIOS options and reset the system.

➔ **Discard Changes and Reset**

Use the **Discard Changes and Reset** option to exit the system without saving the changes made to the BIOS configuration setup program.

➔ **Restore Defaults**

Use the **Restore Defaults** option to load the optimal default values for each of the parameters on the Setup menus. **F3 key can be used for this operation.**

➔ **Save as User Defaults**

Use the **Save as User Defaults** option to save the changes done so far as user defaults.

➔ **Restore User Defaults**

Use the **Restore User Defaults** option to restore the user defaults to all the setup options.

Appendix

A

Regulatory Compliance

DECLARATION OF CONFORMITY

This equipment has been tested and found to comply with specifications for CE marking. If the user modifies and/or installs other devices in the equipment, the CE conformity declaration may no longer apply.

FCC WARNING

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Appendix

B

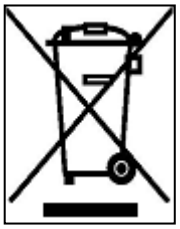
Product Disposal

CAUTION:

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

- Outside the European Union–If you wish to dispose of used electrical and electronic products outside the European Union, please contact your local authority so as to comply with the correct disposal method.
- Within the European Union–The device that produces less waste and is easier to recycle is classified as electronic device in terms of the European Directive 2012/19/EU (WEEE), and must not be disposed of as domestic garbage.



EU-wide legislation, as implemented in each Member State, requires that waste electrical and electronic products carrying the mark (left) must be disposed of separately from normal household waste. This includes monitors and electrical accessories, such as signal cables or power cords. When you need to dispose of your device, please follow the guidance of your local authority, or ask the shop where you purchased the product. The mark on electrical and electronic products only applies to the current European Union Member States.

Please follow the national guidelines for electrical and electronic product disposal.

Appendix

C

BIOS Options

Below is a list of BIOS configuration options in the BIOS chapter.

Appendix

D

Watchdog Timer

NOTE:

The following discussion applies to DOS environment. Contact IEI support or visit the IEI website for specific drivers for other operating systems.

The Watchdog Timer is provided to ensure that standalone systems can always recover from catastrophic conditions that cause the CPU to crash. This condition may have occurred by external EMIs or a software bug. When the CPU stops working correctly, Watchdog Timer either performs a hardware reset (cold boot) or a Non-Maskable Interrupt (NMI) to bring the system back to a known state.

A BIOS function call (INT 15H) is used to control the Watchdog Timer.

INT 15H:

AH – 6FH Sub-function:	
AL – 2:	Sets the Watchdog Timer's period.
BL:	Time-out value (Its unit-second is dependent on the item "Watchdog Timer unit select" in CMOS setup).

Table D-1: AH-6FH Sub-function

Call sub-function 2 to set the time-out period of Watchdog Timer first. If the time-out value is not zero, the Watchdog Timer starts counting down. When the timer value reaches zero, the system resets. To ensure that this reset condition does not occur, calling sub-function 2 must periodically refresh the Watchdog Timer. However, the watchdog timer is disabled if the time-out value is set to zero.

A tolerance of at least 10% must be maintained to avoid unknown routines within the operating system (DOS), such as disk I/O that can be very time-consuming.

NOTE:

When exiting a program it is necessary to disable the Watchdog Timer, otherwise the system resets.

EXAMPLE PROGRAM:

```
; INITIAL TIMER PERIOD COUNTER

;
W_LOOP:
;

        MOV     AX, 6F02H       ;setting the time-out value
        MOV     BL, 30          ;time-out value is 48 seconds
        INT     15H

;
; ADD THE APPLICATION PROGRAM HERE
;

        CMP     EXIT_AP, 1      ;is the application over?
        JNE     W_LOOP          ;No, restart the application

        MOV     AX, 6F02H       ;disable Watchdog Timer
        MOV     BL, 0           ;
        INT     15H

;
; EXIT ;
```

Appendix

E

Error Beep Code

E.1 PEI Beep Codes

Number of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

E.2 DXE Beep Codes

Number of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

NOTE:

If you have any question, please contact IEI for further assistance.

Appendix

F

Hazardous Materials Disclosure

F.1 RoHS II Directive (2015/863/EU)

The details provided in this appendix are to ensure that the product is compliant with the RoHS II Directive (2015/863/EU). The table below acknowledges the presences of small quantities of certain substances in the product, and is applicable to RoHS II Directive (2015/863/EU).

Please refer to the following table.

Part Name	Toxic or Hazardous Substances and Elements									
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (CR(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)	Bis(2-ethylhexyl) phthalate (DEHP)	Butyl benzyl phthalate (BBP)	Dibutyl phthalate (DBP)	Diisobutyl phthalate (DIBP)
Housing	O	O	O	O	O	O	O	O	O	O
Printed Circuit Board	O	O	O	O	O	O	O	O	O	O
Metal Fasteners	O	O	O	O	O	O	O	O	O	O
Cable Assembly	O	O	O	O	O	O	O	O	O	O
Fan Assembly	O	O	O	O	O	O	O	O	O	O
Power Supply Assemblies	O	O	O	O	O	O	O	O	O	O
Battery	O	O	O	O	O	O	O	O	O	O

O: This toxic or hazardous substance is contained in all of the homogeneous materials for the part is below the limit requirement in Directive (EU) 2015/863.

X: This toxic or hazardous substance is contained in at least one of the homogeneous materials for this part is above the limit requirement in Directive (EU) 2015/863.

F.2 China RoHS

此附件旨在确保本产品符合中国 RoHS 标准。以下表格标示此产品中某有毒物质的含量符合中国 RoHS 标准规定的限量要求。

本产品上会附有"环境友好使用期限"的标签，此期限是估算这些物质"不会有泄漏或突变"的年限。本产品可能包含有较短的环境友好使用期限的可替换元件，像是电池或灯管，这些元件将会单独标示出来。

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (CR(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
壳体	O	O	O	O	O	O
印刷电路板	O	O	O	O	O	O
金属螺帽	O	O	O	O	O	O
电缆组装	O	O	O	O	O	O
风扇组装	O	O	O	O	O	O
电力供应组装	O	O	O	O	O	O
电池	O	O	O	O	O	O

O: 表示该有毒有害物质在该部件所有物质材料中的含量均在 SJ/T11364-2014 與 GB/T26572-2011 标准规定的限量要求以下。

X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T11364-2014 與 GB/T26572-2011 标准规定的限量要求。