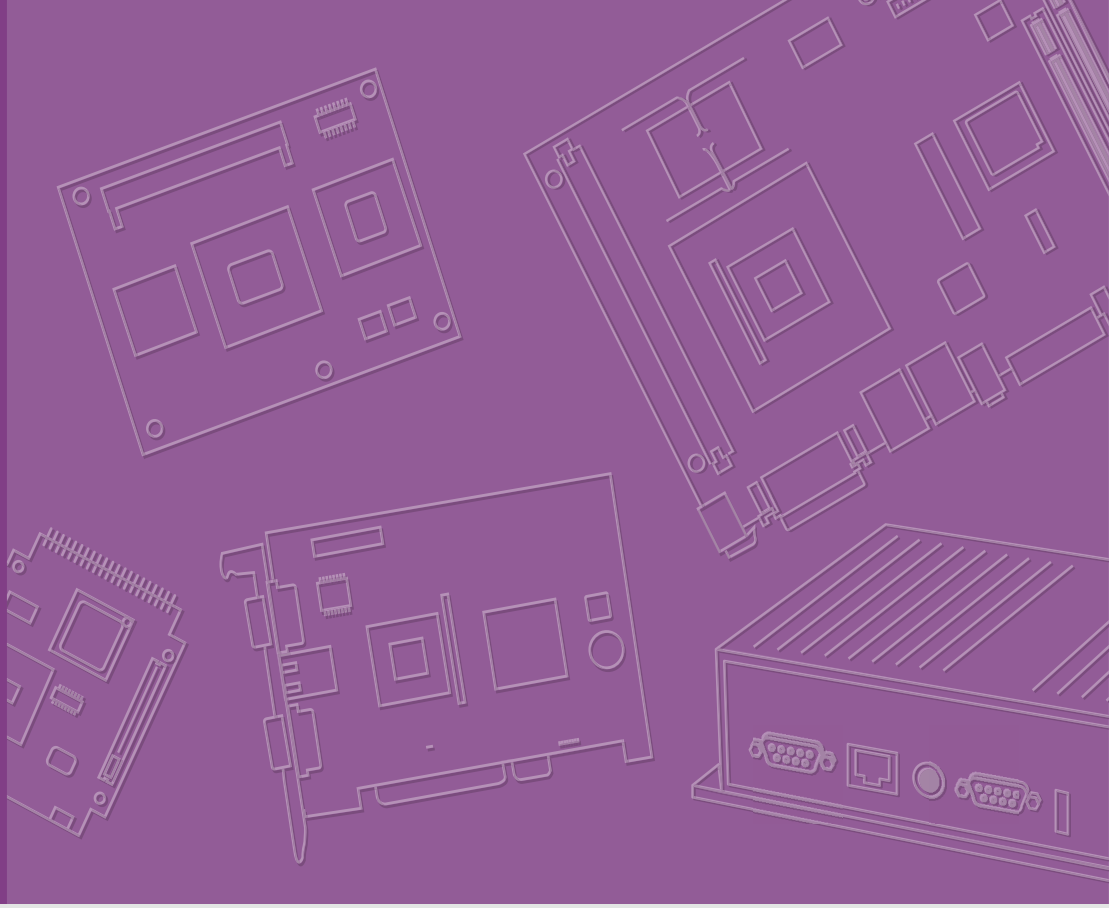

User Manual

# MIO-5373

## MIO-5373 3.5" MI/O-Compact SBC, 8th Gen. Intel® Core™ U-Series (i7/ i5/i3/Celeron®), DDR4, eMMC, HDMI, DP, 48-bit LVDS, 2x GbE, M.2 B Key 2280, DC-in 12-24V, and iManager

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# Acknowledgments



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http://www.advantech.com

For technical support and customer service, visit the Advantech support website at

http://support.advantech.com/

This manual is for MIO-5373.

Part No. 2006537301 Edition 2

Printed in China November 2020

# Product Warranty (2 years)

Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Advantech, or which have been subject to misuse, abuse, accident or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. Please consult your dealer for more details.

If you think you have a defective product, follow these steps:

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages you get when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain an return merchandise authorization (RMA) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

# Declaration of Conformity

### CE

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by electrostatic discharge (ESD) and electromagnetic interference (EMI) leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

### FCC Class B

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his/her own expense.

***Caution!*** *There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manflatterer. Discard used batteries according to the manufacturer's instructions.*

# Technical Support and Assistance

1. Visit the Advantech website at http://support.advantech.com to obtain the latest product information.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

# Packing List

Before installing the card, ensure that the following materials have been shipped:

- 1x MIO-5373 SBC
- 1x SATA Cable 30 cm (11.8 in) (P/N: 1700006291)
- 1x SATA Power Cable 35cm (13.77 in) (P/N: 1700018785)
- 1x Audio JACK*3 Cable 20 cm (7.87 in) (P/N: 1700019584)
- 1x COM RS-232 Cable 20 cm (7.87 in) (P/N: 1700030404-01)
- 1x MIO-5373 Heatsink for 0 ~ 60 °C (32 ~ 140 °F) (P/N: 1960091427N001)
- 1x MIO-5373 Heatsink for -40 ~ 85 °C (-40 ~ 185 °F) (P/N: 1960091427N011)
- 1x Screw Kit (4 sets of screw & stand-off)
- 1x Mini Jumper (P/N: 9689000002)

If any of these items are missing or damaged, contact your distributor or sales representative immediately

# Optional MIOe Module

| Part Number | Description |
|---|---|
| MIOe-210-D6A1E | 4x RS232/422/485, 2 x RS422/485, 8-bit GPIO |
| MIOe-220-B3A1E | 3x Intel® Gigabit Ethernet with PCIe Switch |
| MIOE-260L-00A1 | Dual Intel GbE with M.2 B-key & F/S miniPCIe |
| MIOe-3674-AE[1] | 4-port PoE ports MIOe Module |
| MIOe-3680-AE | 2-Port CAN-Bus MIOe Module with Isolation Protection |
| MIOE-PWR1-00A1E | 12-24V Power Module |
| MIOE-PWR2-00A1E | 9-36V Power Module |

[1] Supported with customized BIOS

# Optional Accessories

| Part Number | Description |
|---|---|
| 1970004423N000 | Heat spreader for single layer display HDMI connector (optional) |
| 1970004423N010 | Heat spreader for dual layer display HDMI + DP connector |
| 1960090264N000 | Bracket for M.2 2280 to M.2 3042 |

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# Chapter 1

## General Information

This chapter details background information regarding MIO-5373.

- Introduction
- Specifications
- Block Diagram
- Board Layout and Dimensions

# 1.1 Introduction

Advantech's MIO-5373 3.5" SBC w/ MIOe is powered by 8th Gen. Intel® Core i7/i5/i3/Celeron processors. It offers low power features, high performance computing, and multimedia capabilities. MIO-5373 supports Advantech's iManager, SW APIs, and WISE-PaaS/DeviceOn to remotely monitor and control system operation effectively.

MIO-5373 adopts the latest 64-bit, Quad-core processors built on 14nm process technology for improvements in CPU processing, graphics, security and I/O flexibility.

MIO-5373 is equipped with Intel® latest generation graphics core with DX12, OGL4.4, HW Encode:H.264 & MPEG2, HW Decode:H.264 & MPEG2 encoding/decoding and supports triple simultaneous displays by 48-bit LVDS/eDP+HDMI+DP, dual-channel 2400MHz DDR4 memory (Max. 32GB), M.2 B-Key 2280 (supports NVMe), and DC-in 12~24V.

# 1.2 Specifications

## 1.2.1 Functional Specifications

- **Processor: 8th Gen. Intel® Core™ U-series**
  - Intel® Core™ i7-8665UE (Quad-Core, 1.70GHz)
  - Intel® Core™ i5-8365UE (Quad-Core, 1.60GHz)
  - Intel® Core™ i3-8145UE (Dual-Core, 2.20GHz)
- **LLC**
  - Intel® Core™ i7-8665UE: 2MB
  - Intel® Core™ i5-8365UE: 2MB
  - Intel® Core™ i3-8145UE: 2MB
- **Advanced Technologies**

  * Intel® Turbo Boost Technology 2.0[2] (i5/i7 series only)
  * Intel® Advanced Vector Extensions 2.0 (Intel® AVX2)
  * Intel® Hyper-Threading Technology
  * Intel® Active Management Technology 11.0 (Intel® AMT 11.0, i5/i7 series only)
  * Intel® Trusted Execution Technology (Intel® TXT)
  * Intel® 64 Architecture
  * Intel® Virtualization Technology (Intel® VT)
  * Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI)
  * Enhanced Intel SpeedStep® Technology

- **I/O Interface of Platform Controller Hub**
  - SATA
    2x SATA 3.0:
    *Integrated Serial ATA Host Controller
    *Data transfer rates up to 6.0 Gb/s (600MB/s)
    *Integrated AHCI controller
  - USB
    4x rear I/O USB 3.1 ports at coastline
    2x internal USB 2.0 ports
  - Power Management

- Full ACPI (Advanced Configuration and Power Interface) with ATX mode: C0-C7 support; C8, C9, C10 no support
- Support S0, S3, S4, S5
- Support Wake on LAN
- Enhanced Intel® SpeedStep® Technology

■ **System Memory Support**

- Technology: DDR4-2400MT/s
- Max. Capacity: 32GB
- Channel/Socket:
  *Dual Channel/Dual Socket DDR4 (5.2 mm)
  *Dual Channel/Dual Socket DDR4 (9.2 mm)
- ECC Support: N/A

■ **Integrated Graphics Controller**

- Controller: Intel® WHL-U SoC integrated
- Max. Frequency: i7-8665UE (400 MHz)
- Base Frequency: i7-8665UE (550 MHz)
- 3D/HW Acceleration:
  DX12, OGL4.4
  HW Encode: H.264, MPEG2
  HW Decode: H.264, MPEG2
- Multiple Display: Triple simultaneous displays by 48-bit LVDS/ eDP+HDMI+DP
- LCD:
  LVDS Dual Channel 48-bit up to 1920 x 1200
  Option eDP1.4 up to 4096x2304@60Hz
- HDMI/DP:
  1x Port HDMI1.4 up to 4096x2160@30/24Hz
  1x Port DP1.2 up to 4096x2306@60Hz

■ **Gigabit Ethernet**

- Controller:
  LAN1: Intel® i219
  LAN2: Intel® i210-IT
- Compliant with IEEE 802.3, IEEE 802.3u, IEEE 802.3z, IEEE 802.ab
- Speed: 10/100/1000 Mbps
- LAN LED:
  Link: Green (100Mbps)/Orange (1000Mbps)
  Active: Green (flash)
- Support wake on LAN

■ **Peripheral Interface**

- MIOe Unified Expansion: 4 PCIex1, 1 PCIex4, USB2.0, LPC, SMBus, Line-out, 12V/5V Power supply
- COM Port:
  2x RS-232/422/485
  2x GPIO 8b (default) or 2 x RS-232 (*by request)
- 16-bit GPIO
- 1 SMBus / $I^2C$ channel from iManager
- Watchdog timer: 65536 level, 0~65535 sec
- 1x M.2 E-key 2230
- 1x M.2 B-key 2280 (SATA or NVMe PCIex2), 3042 LTE module (support USB 2.0 only), optional M-key 2280 NVMe PCIex4

- **High Definition Audio**
  - Intel® High Definition Audio Interface
  - High Definition Audio Codec with Realtek proprietary loss-less content protection technology
  - Supports 1x Line-input, 1x Line output, 1x Mic-input
- **BIOS: AMI EFI 256Mbit**
- **Security: TPM2.0, supported by UEFI mode only**

### 1.2.2 OS Support

MIO-5373 supports Win10 64-bit (UEFI mode only).

For further information regarding OS support for MIO-5373, please visit Advantech's website or contact our technical support center.

http://support.advantech.com.tw/

### 1.2.3 Mechanical Specifications

- **Dimensions:** 146 x 102 mm (5.7 x 4 in)
- **Height:** Top: 25.3 mm (.996 in), PCB: 2.0 mm (.07 in); bottom: 10.51 mm (10.51 in)
- **Weight:** 0.67 kg/1.47 lb (reference weight of total package)

### 1.2.4 Electrical Specifications

- **Power Requirement**
  - Supply Voltage: Vin: 12V-24V +/- 10%
  - Connector: ATX 2x2-pin, optional: DC-Jack*
  - Power Management: AT, ATX
- **Power Consumption**
  - Max.:
    i7-8665UE: 65.59W (12V)/74.06W (24V)
    i5-8365UE: 71.28W (12V)/74.04W (24V)
    i3-8145UE: 35.70W (12V)/38.68W (24V)
  - Typical: Idle mode in Windows 10
    i7-8665UE: 6.68W (12V)/8.71W (24V)
    i5-8365UE: 7.55W (12V)/7.55W (24V)
    i3-8145UE: 7.03W (12V)/8.18W (24V)
- **Power Consumption Conditions**
  - Max. load: Measures the maximum current value the system is under during maximum loading (CPU: Top speed, RAM, and Graphic: Full loading)
  - Idle mode: Measures the current value when the system is in windows mode without running any programs
- **RTC Battery**
  - Typical Voltage: 3.0 V
  - Normal discharge capacity: 210 mAh

### 1.2.5 Environmental

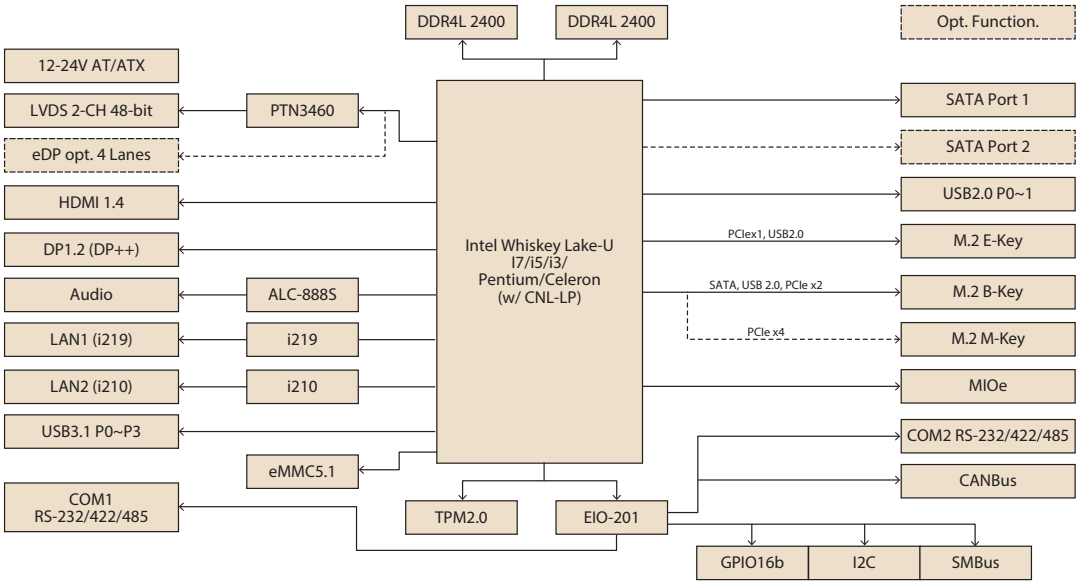
- **Temperature**
  - Operating:
    Standard: 0 ~ 60 °C (32 ~ 140 °F)
    Extend: -40 ~ 85 °C (-40 ~ 185 °F)
  - Storage: -40 ~ 85 °C (-40 ~ 185 °F)

- **Humidity**
  - Operating: 40 °C (104 °F) @ 95% relative humidity, non-condensing
  - Storage: 60 °C (140 °F) @ 95% relative humidity, non-condensing
- **Vibration Resistance:** 3.5Grms

[1] Not supported by default. Please contact Advantech if this function is needed.

[2] Thermal conditions need to be considered when setting maximum frequency.

## 1.3 Block Diagram




## 1.4 Board Dimensions

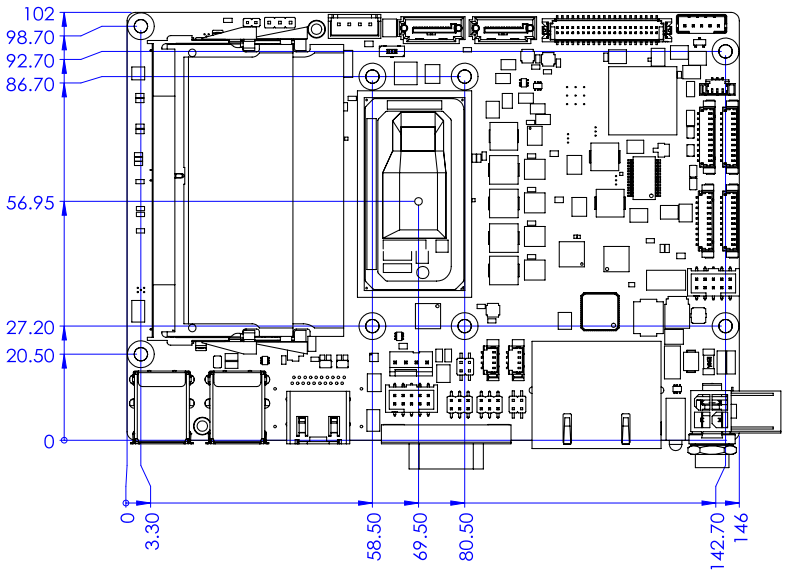



**Figure 1.1 MIO-5373 Mechanical Diagram (Top Side)**

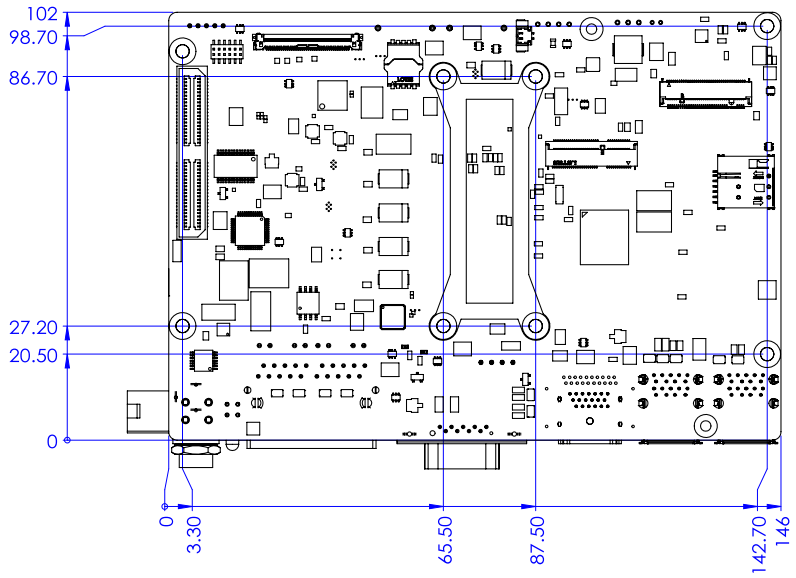



**Figure 1.2 MIO-5373 Mechanical Diagram (Bottom Side)**

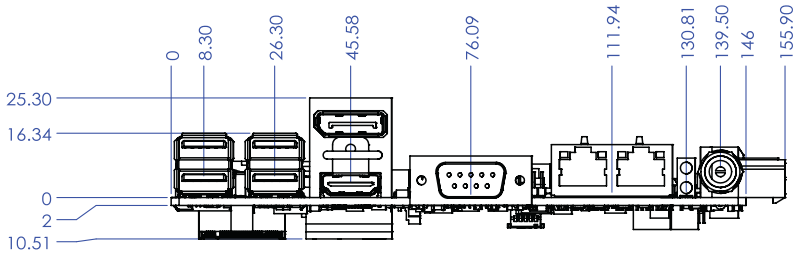



**Figure 1.3 MIO-5373 Mechanical Diagram (Coastline)**

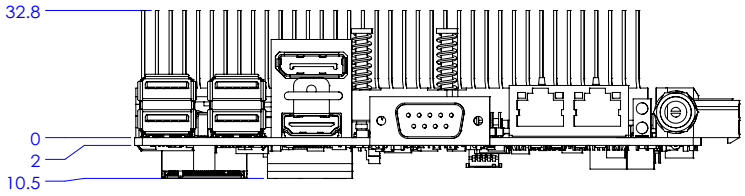



**Figure 1.4 MIO-5373 Mechanical Diagram (with Heatsink)**

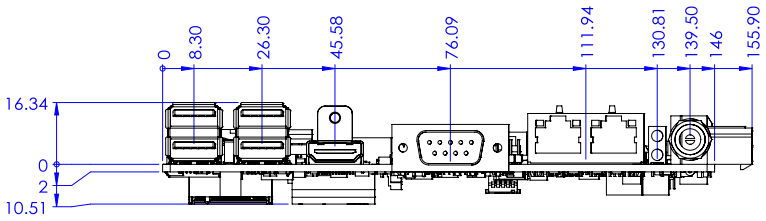



**Figure 1.5 MIO-5373 Mechanical Drawing for Single Layer Display HDMI Connector (Coastline)**

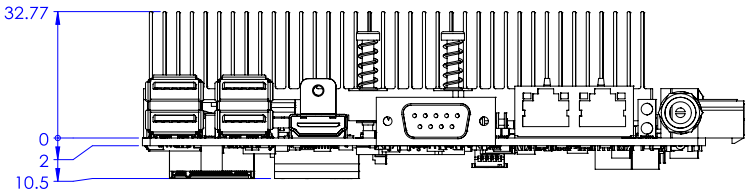



**Figure 1.6 MIO-5373 Mechanical Drawing for Single Layer Display HDMI Connector (with Heatsink)**

# Chapter 2

## Installation

This chapter explains the setup procedures of the MIO-5373 hardware, including instructions on setting jumpers and connecting peripherals, switches and indicators. Be sure to read all safety precautions before you begin the installation procedure.

## 2.1 Jumpers & Switches

MIO-5373 has a number of jumpers that allow you to configure your system to suit your application. The table below lists the functions of the various jumpers.

| Table 2.1: Jumpers & Switches | |
|---|---|
| J1 | AT/ATX mode selection |
| J2 | RI# 5V/12V selection pin for CN9 |
| J3 | Panel voltage selection |
| J4 | LVDS JEIDA and VESA mode selection |
| SW1 | Clear CMOS |

## 2.2 Connectors

Onboard connectors link the MIO-5373 to external devices such as hard disk drives, a keyboard, or floppy drives. The table below lists the function of each of the board's connectors.

**Table 2.2: Connector**

| Label | Function |
|---|---|
| CN1 | DDR4 SODIMM 260P/H5.2mm |
| CN2 | DDR4 SODIMM 260P/H9.2mm |
| CN3 | DC Input Connector |
| CN5 | RTC Battery Connector |
| CN8 | Power/LED/Case Open/Buzzer Connector |
| CN9 | COM port Connector (RS232+RS422+RS485) |
| CN10 | COM port Connector (RS232+RS422+RS485) |
| CN11 | RJ45 Connector (2 port) |
| CN12 | Inverter Connector |
| CN13 | LVDS Connector |
| CN14 | eDP Connector |
| CN15 | HDMI and DP++ Connector |
| CN16 | Key E Connector |
| CN17 | Key M and Key B (option) Connector |
| CN20 | SIM Card Connector |
| CN22 | USB 3.1 Connector (2 ports) |
| CN23 | USB 3.1 Connector (2 ports) |
| CN24 | Internal USB Connector |
| CN25 | HDD Power Connector |
| CN26 | HDD Connector |
| CN27 | HDD Connector |
| CN28 | GPIO/RS232 Connector |
| CN29 | Audio Connector |
| CN30 | GPIO/RS232 Connector |
| CN30A1 | MIOe Connector |
| CN31 | I2C Bus Connector |
| CN32 | System FAN Connector |
| CN35 | CANBus Connector |
| CN36 | SMBus Connector |
| CN37 | DC input Connector (Adapter) |

## 2.3 Connector Locations

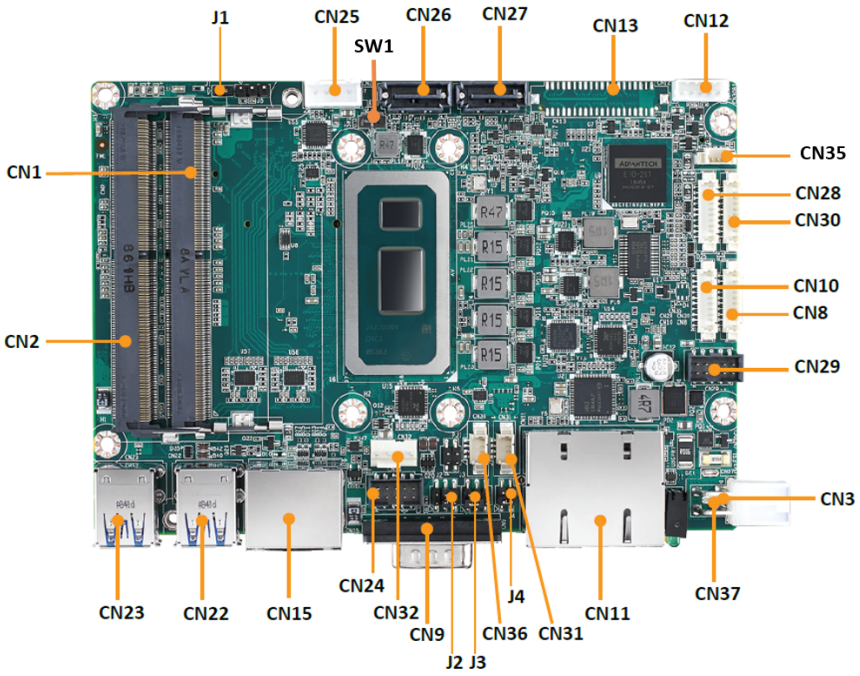



**Figure 2.1 MIO-5373 Connector Locations Diagram (Top Side)**

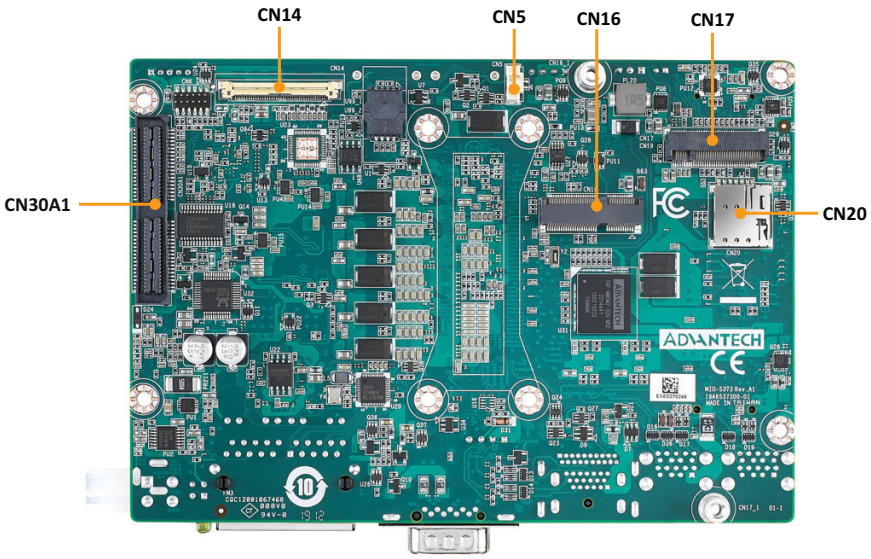



**Figure 2.2 MIO-5373 Connector Locations Diagram (Bottom Side)**

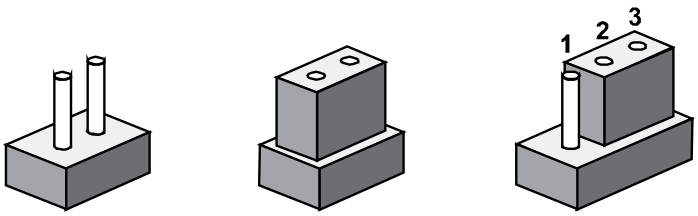
**Figure 2.3 MIO-5373 Connector Locations Diagram (Coastline)**

**Figure 2.4 MIO-5373 Connector Locations with Single Layer HDMI (Coastline)**

## 2.4 Setting Jumpers

You may configure your card to match the needs of your application by setting jumpers. A jumper is a metal bridge used to close an electric circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper, connect the pins with the clip. To “open” a jumper, remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case, connect either pins 1 and 2, or 2 and 3.

The jumper settings are schematically depicted in this manual as follows:

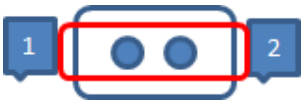



**open** **closed** **closed 2-3**

A pair of needle-nose pliers may be helpful when working with jumpers. If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes. Generally, you only need a standard cable to make most connections.

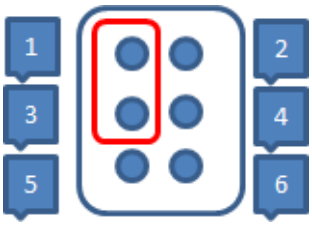
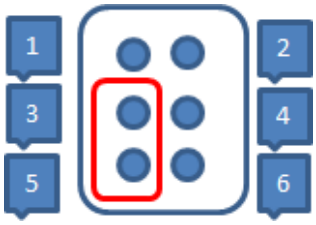
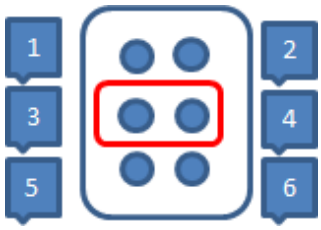
## 2.5 Jumper Settings

### 2.5.1 J1: ATX/AT Mode Selection

| Function | Jumper Setting |
|---|---|
| AT Mode (Default) |  |
| ATX Mode |  |

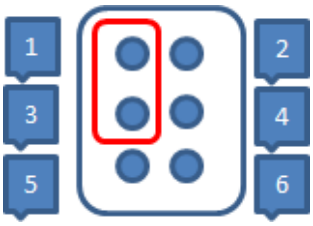
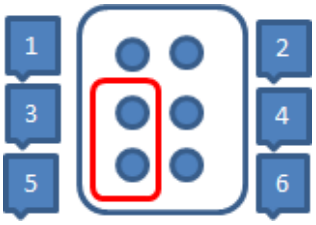
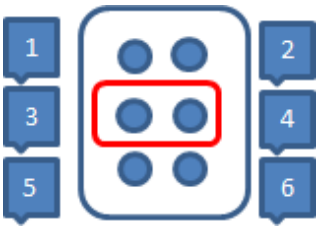
| Pin | Signal Pin Definition |
|---|---|
| 1 | AT_DET# |
| 2 | GND |

### 2.5.2 J2: RI# 5V/12V Selection Pin for CN9

| Function | Jumper Setting |
|---|---|
| RI# Voltage Setting: +V5 |  |
| RI# Voltage Setting: +V12 |  |
| RI# Voltage Setting: RI# (Default) |  |

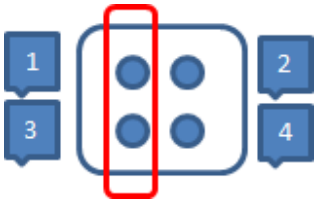
| Pin | Signal Pin Definition |
|---|---|
| 1 | +V5 |
| 2 | CN9_RI# |
| 3 | COM_RI# |
| 4 | CN9_RI# |
| 5 | +V12 |
| 6 | CN9_RI# |

### 2.5.3 J3: Panel Voltage Selection

| Function | Jumper Setting |
|---|---|
| Panel Voltage Setting: +V3.3(Default) |  |
| Panel Voltage Setting: +V5 |  |
| Panel Voltage Setting: +V12 |  |

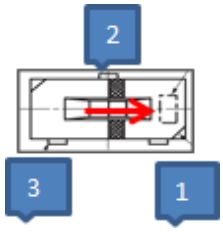
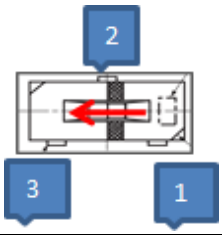
| Pin | Signal Pin Definition |
|---|---|
| 1 | +V3.3 |
| 2 | NC |
| 3 | +V_CH7511B_LCD |
| 4 | +V12 |
| 5 | +V5 |
| 6 | NC |

### 2.5.4 J4: JEIDA and VESA Mode Selection

| Function | Jumper Setting |
|---|---|
| JEIDA mode Setting: +V3.3 |  |
| VESA mode Setting: GND (Default) |  |

| Pin | Signal Pin Definition |
|---|---|
| 1 | LVDS1_VCON |
| 2 | LVDS1_VCC |
| 3 | GND |
| 4 | NC |

### 2.5.5 SW1: Clear CMOS

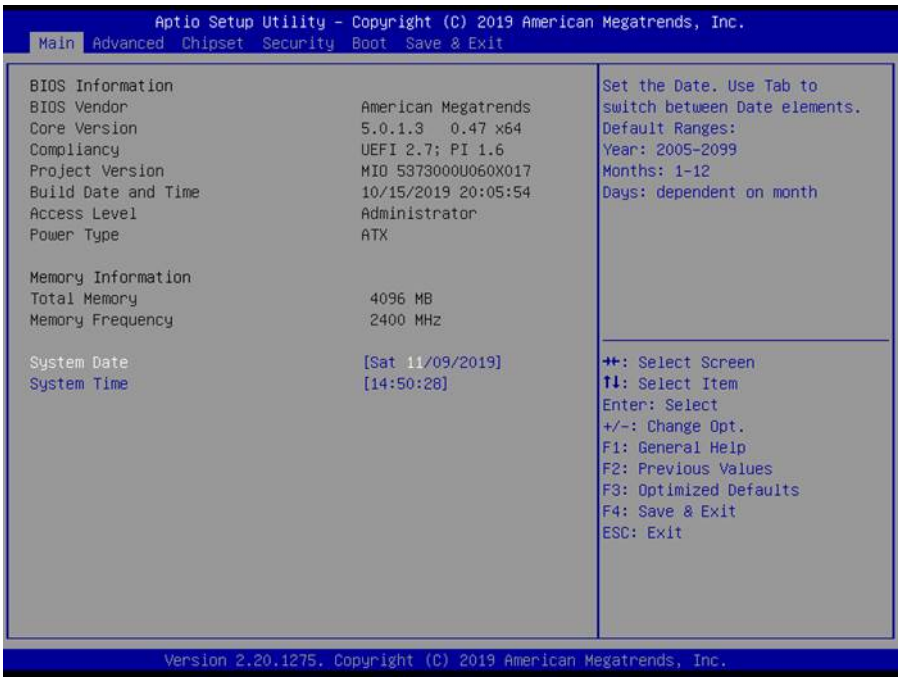
| Function | Jumper Setting |
|---|---|
| Keep COMS Data (Default) |  |
| Clear CMOS Date |  |

| Pin | Signal Pin Definition |
|---|---|
| 1 | RTC_a_RST# |
| 2 | RTC_RST# |
| 3 | GND |

# Chapter 3

## AMI BIOS Setup

AMI BIOS has been integrated into numerous of motherboards for decades. With the AMI BIOS Setup program, you can modify BIOS settings and control the various system features. This chapter describes the basic navigation of the MIO-5373 BIOS setup screens.



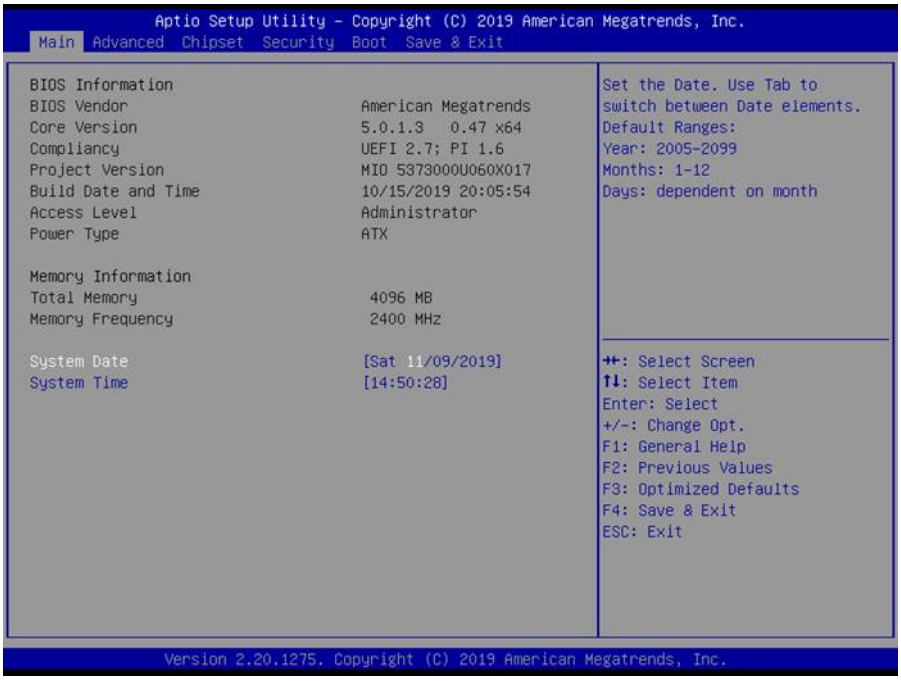

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configurations. This information is stored in battery-backed CMOS so it retains the setup information when the power is turned off.

# 3.1 Entering Setup

Turn on the computer and check for the patch code. If there is a number assigned to the patch code, it means that the BIOS supports your CPU. If there is no number assigned to the patch code, please contact an Advantech application engineer to obtain an up-to-date patch code file. This will ensure that your CPU's system status is valid. After ensuring that you have a number assigned to the patch code, press <DEL> and you will immediately be allowed to enter Setup.

## 3.1.1 Main Setup

When you first enter the BIOS Setup Utility, you will encounter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



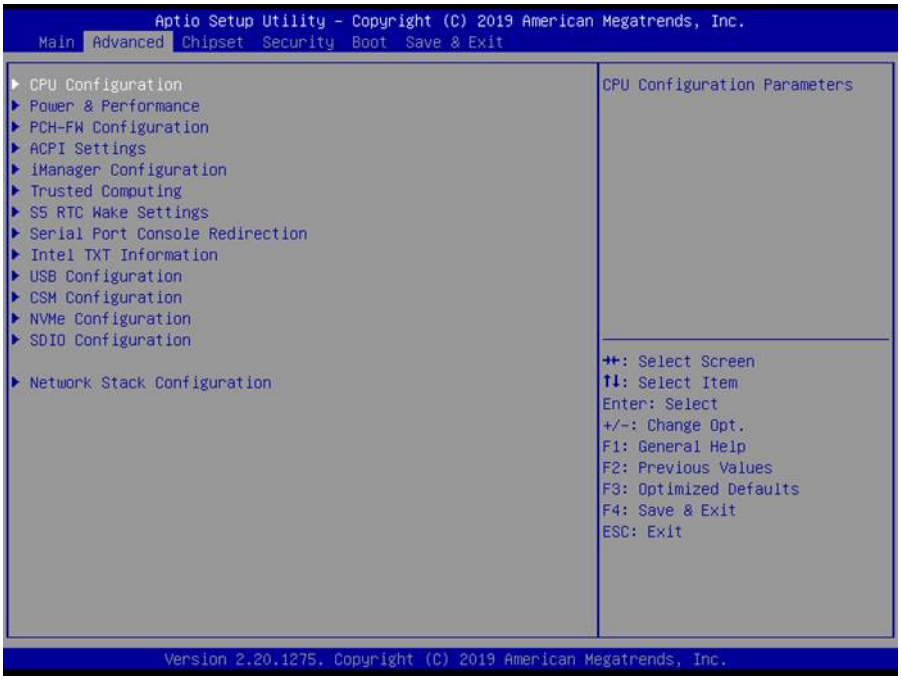

The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the key legend.

Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

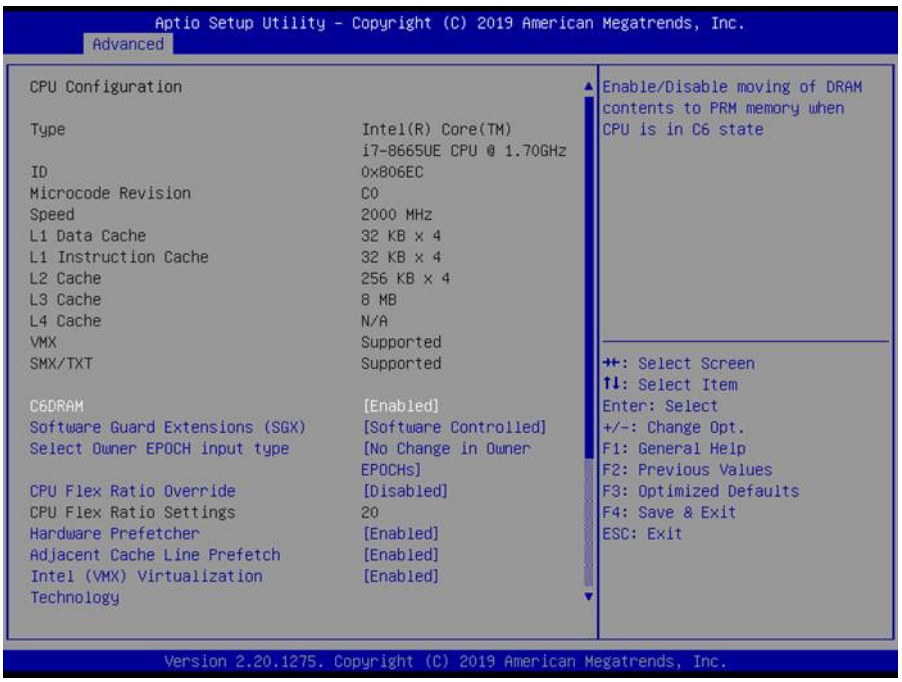
- **System Time / System Date**
  Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

### 3.1.2 Advanced BIOS Features Setup

Select the Advanced tab from the MIO-5373 setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screens are shown below. The sub menus are described on the following pages.



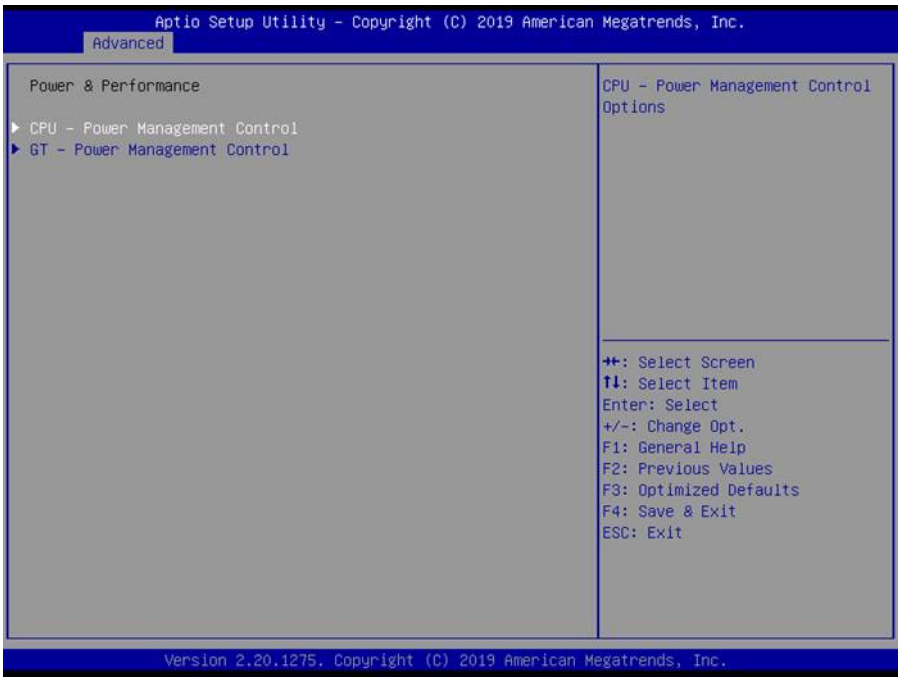

#### 3.1.2.1 CPU Configuration




- **C6DRAM**
  Enable/Disable moving of dram contents to PRM memory when CPU is in C6 state.

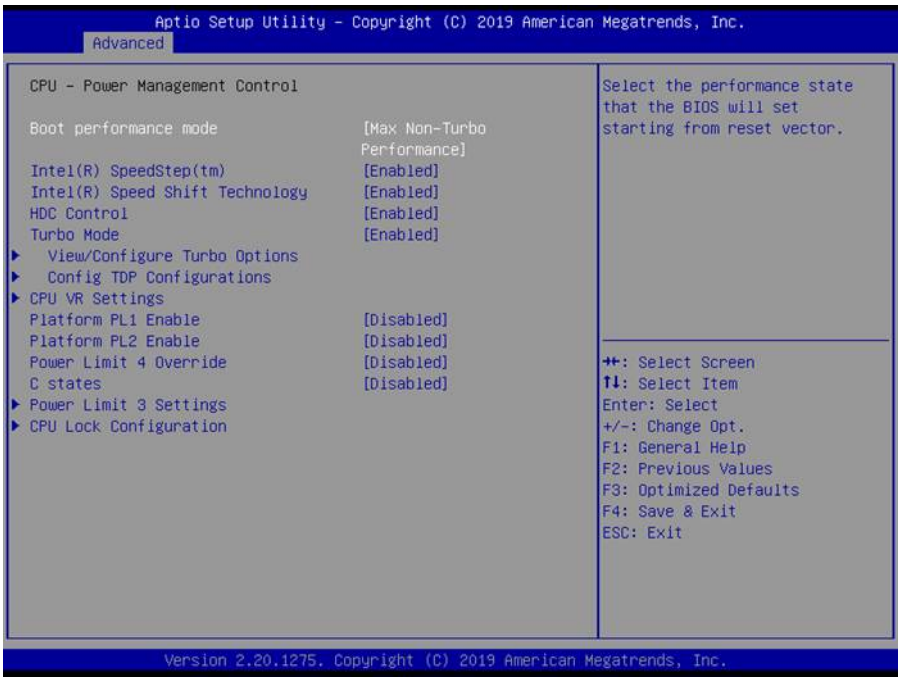
- **SW Guard Extension (SGX)**
  Enable/Disable Software Guard Extensions (SGX).
- **Select Owner EPOCH Input Type**
  Choose Owner EPOCH modes.
- **CPU Flex Ratio Override**
  Enable/Disable CPU Flex Ratio Programming.
- **Hardware Prefetcher**
  This item allows users to enable or disable the hardware prefetcher feature.
- **Adjacent Cache Line Prefetch**
  This item allows users to enable or disable the adjacent cache line prefetch feature.
- **Intel (VMX) Virtualization Technology**
  When Enabled, a VMM can utilize the additional hardware capability provided by Vanderpool Technology.
- **Active Processor Cores**
  This item allows users to set how many processor cores should be active.
- **AES**
  Enable/Disable AES (Advanced Encryption Standard).
- **MachineCheck**
  Enable/Disable Machine Check.
- **MonitorMWait**
  Enable/Disable MonitorMWait.
- **Intel Trusted Execution Technology**
  Enables utilization of additional hardware capability provided by Intel® Trusted Execution Technology.

### 3.1.2.2 Power & Performance



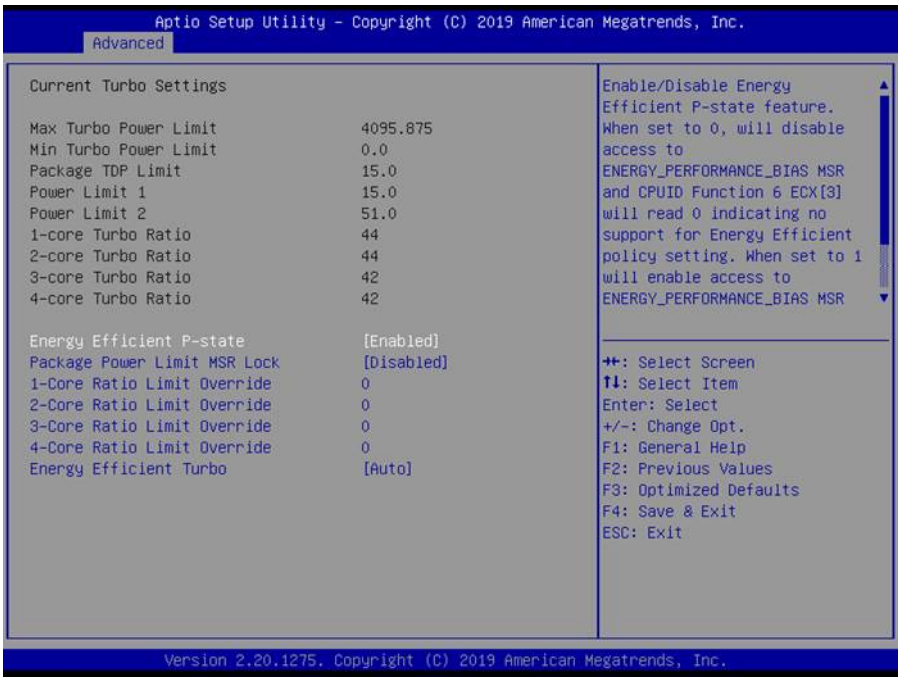

- **CPU - Power Management Control**
  CPU - Power Management Control Options.
- **GT - Power Management Control**
  GT - Power Management Control Options.

### CPU - Power Management Control



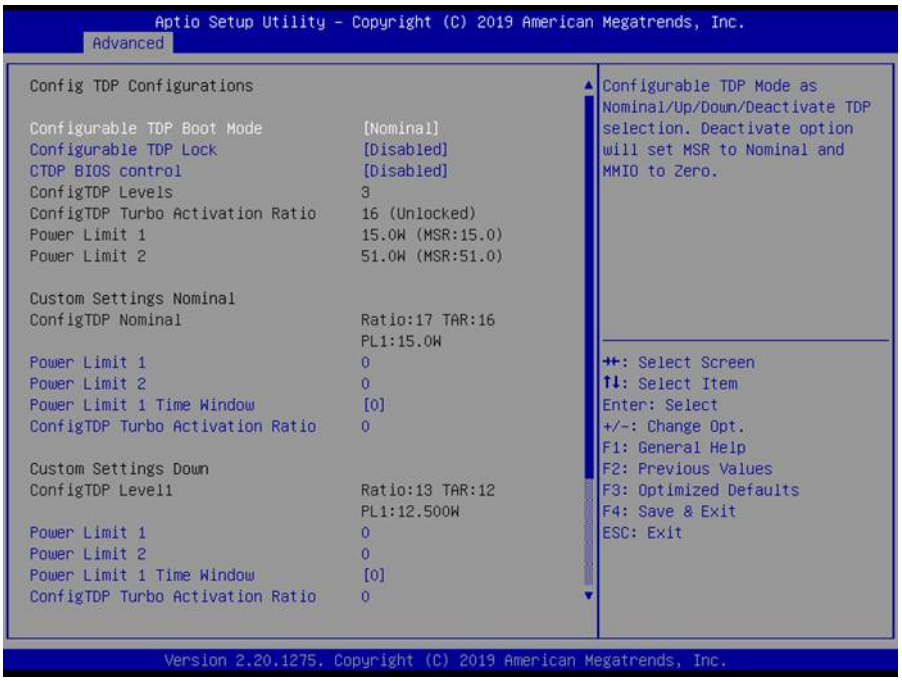

- **Boot Performance mode**
  Select the performance state that the BIOS will set before OS handoff.
- **Intel® SpeedStep™**
  Allows more than two frequency ranges to be supported.
- **Intel® Speed Shift Technology**
  Enable/Disable Intel® Speed Shift Technology support.
- **HDC Control**
  Enable/Disable Intel HDC.
- **Turbo Mode**
  Enable/Disable processor turbo mode.
- **View/Configure Turbo Options**
  View and Configure Turbo Options.
- **Config TDP Configuration**
  Config TDP Configurations.
- **CPU VR Setting**
  CPU CR Settings.
- **Platform PL1 Enable**
  Enable/Disable Platform Power Limit 1 programming.
- **Platform PL2 Enable**
  Enable/Disable Platform Power Limit 1 programming.
- **Power Limit 4 Override**
  Enable/Disable Power Limit 4 override.
- **C states**
  Enable/Disable CPU Power Management.
- **PowerLimit 3 Settings**
  Power Limit 3 Settings.
- **CPU Lock Configuration**
  CPU Lock Configuration.

### View/Configure Turbo Options




- **Energy Efficient P-state**
  Enable/Disable Energy Efficient P-state feature.
- **Package Power Limit MSR Lock**
  Enable/Disable locking of Package Power Limit settings.
- **Energy Efficient Turbo**
  Enable/Disable Energy Efficient Turbo feature.

### Config TDP Configurations




- **Configurable TDP Boot Mode**
  Configurable TDP Mode as Nominal/Up/Down/Deactivate TDP selection.
- **Configurable TDP Lock**
  Configurable TDP Mode Lock sets the Lock bit.
- **CTDP BIOS control**
  Enables CTDP control via runtime ACPI BIOS method.

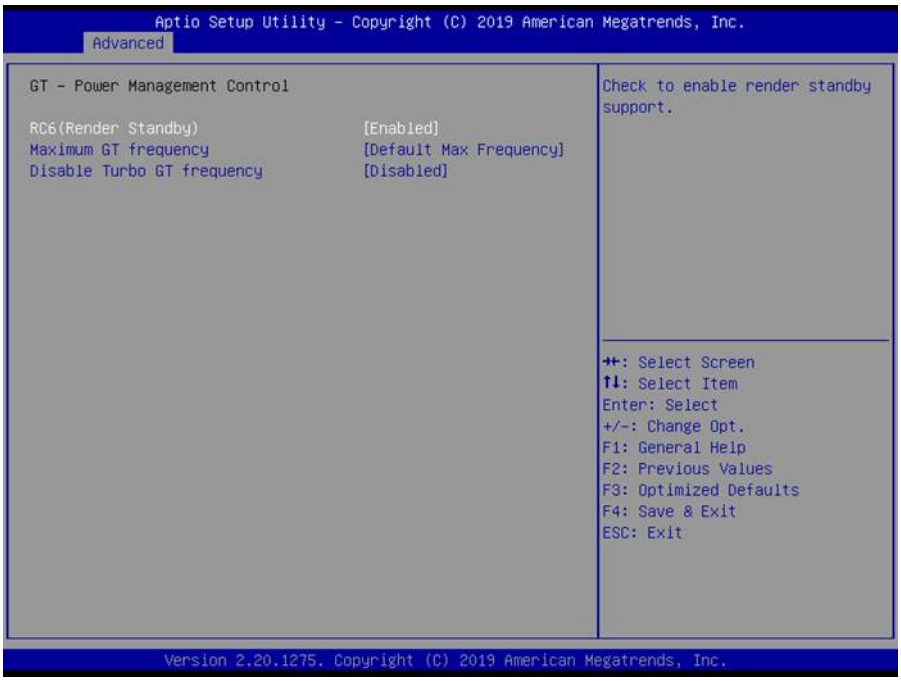
### Power Limit 3 Settings


- **Power Limit 3 Override**
  Enable/Disable Power Limit 3 override.

### CPU Lock Configuration

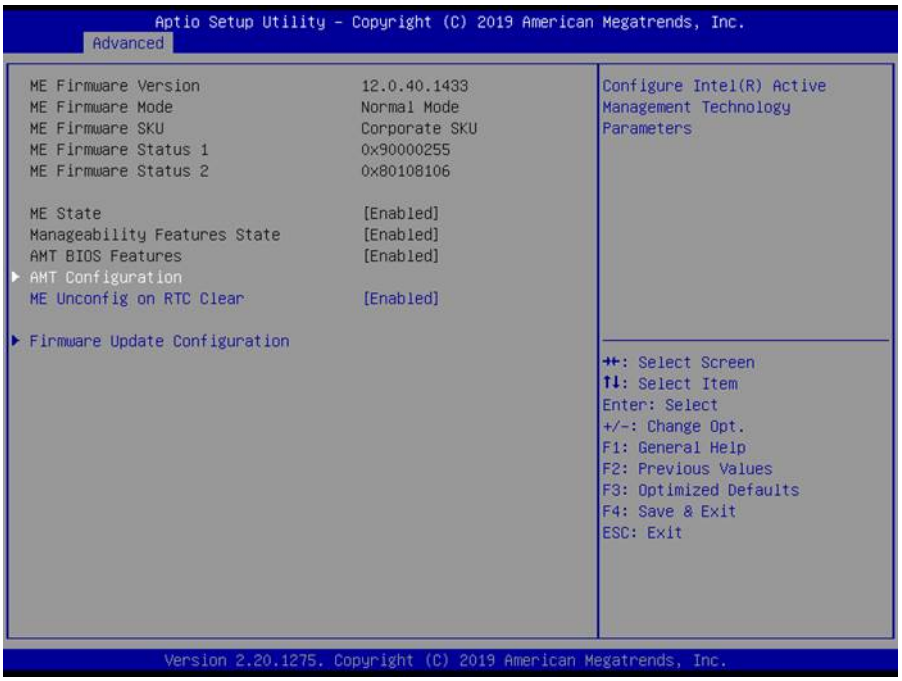

- **CFG Lock**
  Configure MSR 0xE2[15], CFG Lock bit.
- **Overclocking Lock**
  Enable/Disable Overclocking Lock (BIT 20) in FLEX_RATIO(194) MSR.

### GT - Power Management Control



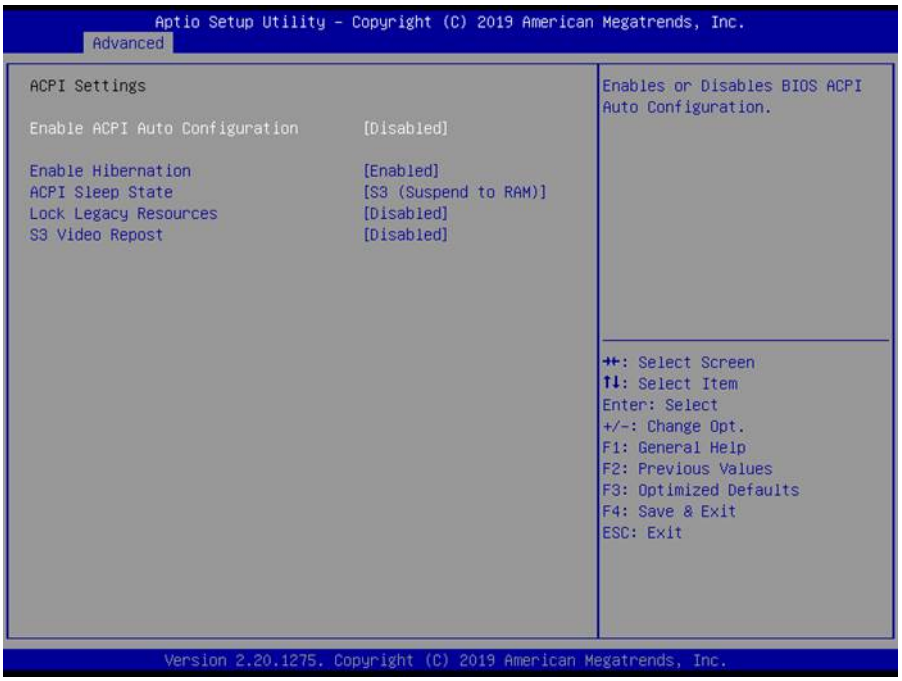

- **RC6(Render Standby)**
  Check to enable render standby support.
- **Maximum GT Frequency**
  Maximum GT frequency limited by user.
- **Disable Turbo GT Frequency**
  Enabled/Disabled Turbo GT frequency.

### 3.1.2.3 PCH-FW Configuration



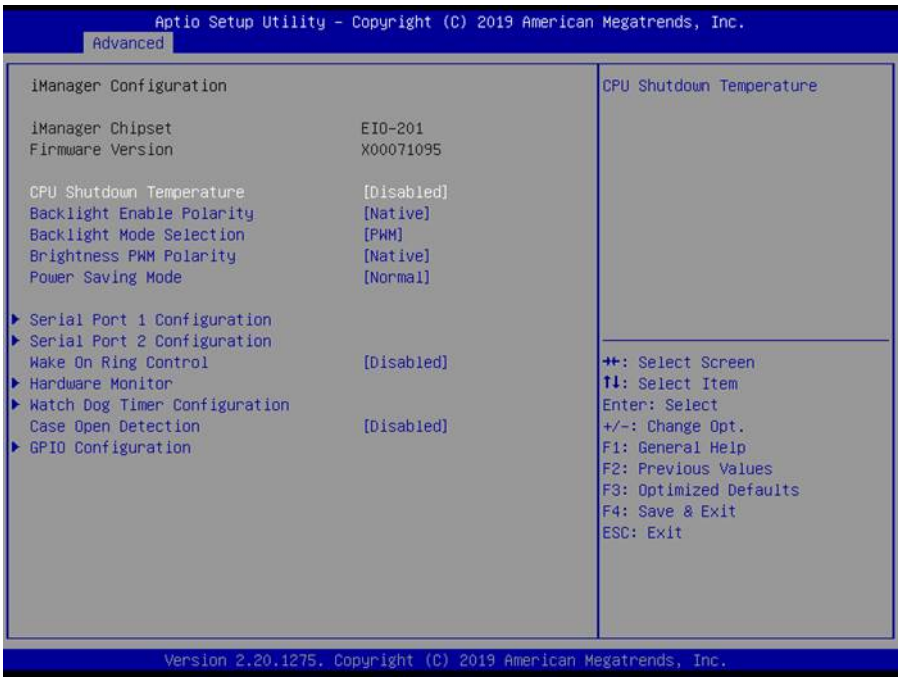

- **ME State**
  When Disabled ME will be put ME into Temporarily Disabled Mode.
- **Manageability Features State**
  Enable/Disable Intel® Manageability features.
- **AMT BIOS Features**
  When disabled, AMT BIOS Features are no longer supported and user is no longer able to access MEBx setup.
- **AMT Configuration**
  Configure Intel® Active Management Technology Parameters.
- **ME Unconfig on RTC Clear**
  When Disabled, ME will not be unconfigured on RTC Clear.
- **Firmware Update Configuration**
  Configure Management Engine Technology Parameters.

### 3.1.2.4 ACPI Settings



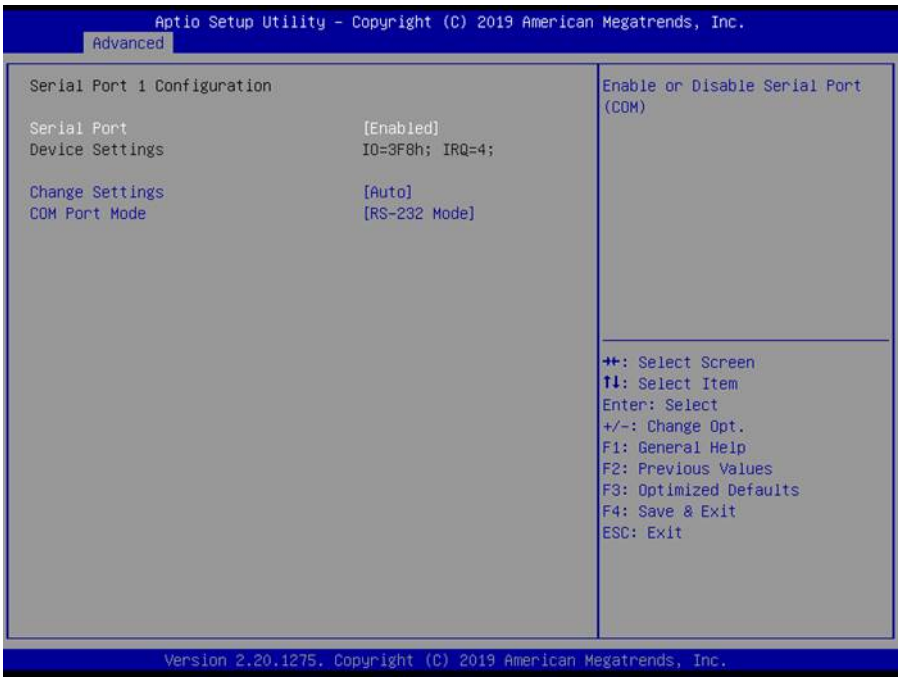

- **Enable ACPI Auto Configuration**
  Enable or disable BIOS ACPI auto configuration.
- **Enable Hibernation**
  Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
- **ACPI Sleep State**
  Select the highest ACPI sleep state the system will enter when the SUSPEND-button is pressed.
- **Lock Legacy Resources**
  Enables or Disables Lock of Legacy Resources.
- **S3 Video Repost**
  Enable or Disable S3 Video Repost.

### 3.1.2.5 iManager Configuration



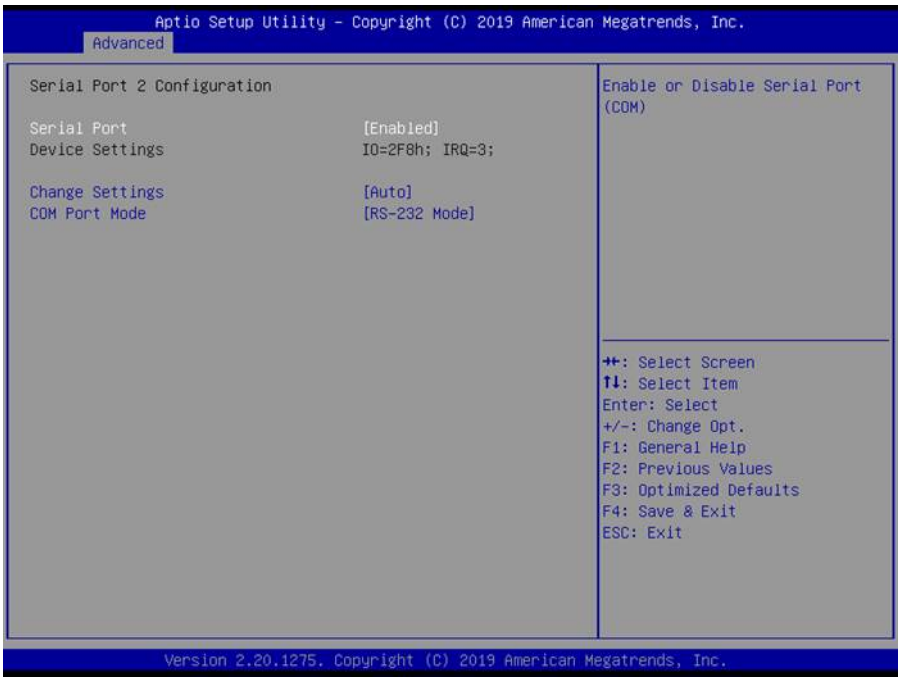

- **CPU Shutdown Temperature**
  Enable/Disable CPU Shutdown Temperature.
- **Backlight Enable Polarity**
  Switch Backlight Enable Polarity for Native or Invert.
- **Backlight Mode Selection**
  Switch Backlight Control to PWM or DC mode.
- **Brightness PWM Polarity**
  Switch Brightness PWM Polarity for Native or Invert.
- **Power Saving Mode**
  Enable/Disable power saving mode.
- **Serial Port 1 Configuration**
  Set Parameters of Serial Port 1.
- **Serial Port 2 Configuration**
  Set Parameters of Serial Port 2.
- **Wake On Ring Control**
  Enable/Disable Wake on Ring Function.
- **Hardware Monitor**
  Monitor hardware Status.
- **Watch Dog Timer Configuration**
  Watch Dog Timer Configuration Page.
- **Case Open Detection**
  Enable or Disable Case Open Detect Function.
- **GPIO Configuration**
  GPIO Configuration Settings.

### Serial Port 1 Configuration



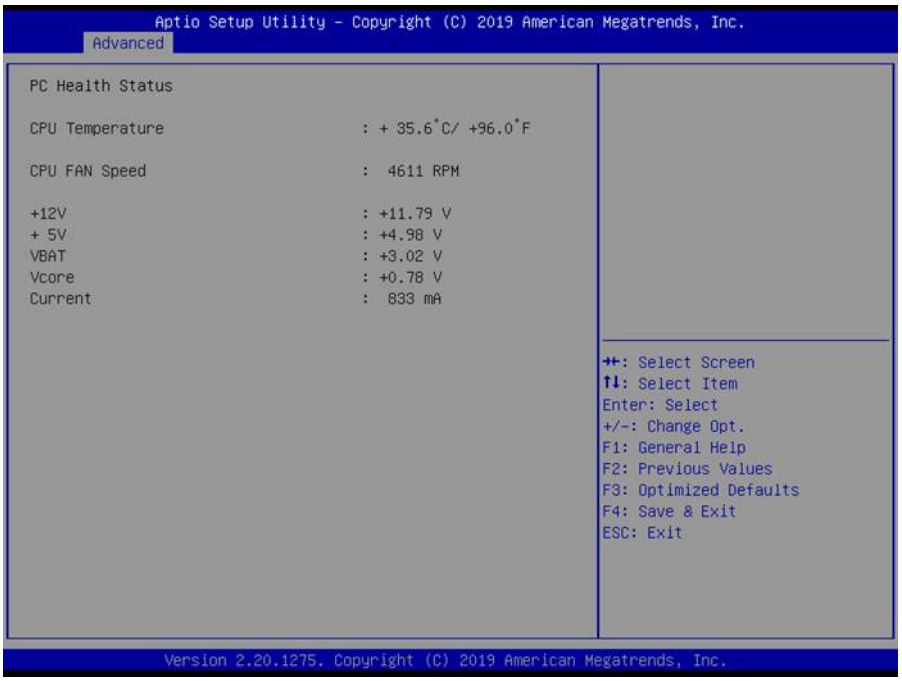

- **Serial Port**
  Enable or Disable Serial Port (COM).
- **Change Settings**
  Select an optimal settings for Super I/O device.
- **COM Port Mode**
  COM Port Mode Select.

### Serial Port 2 Configuration

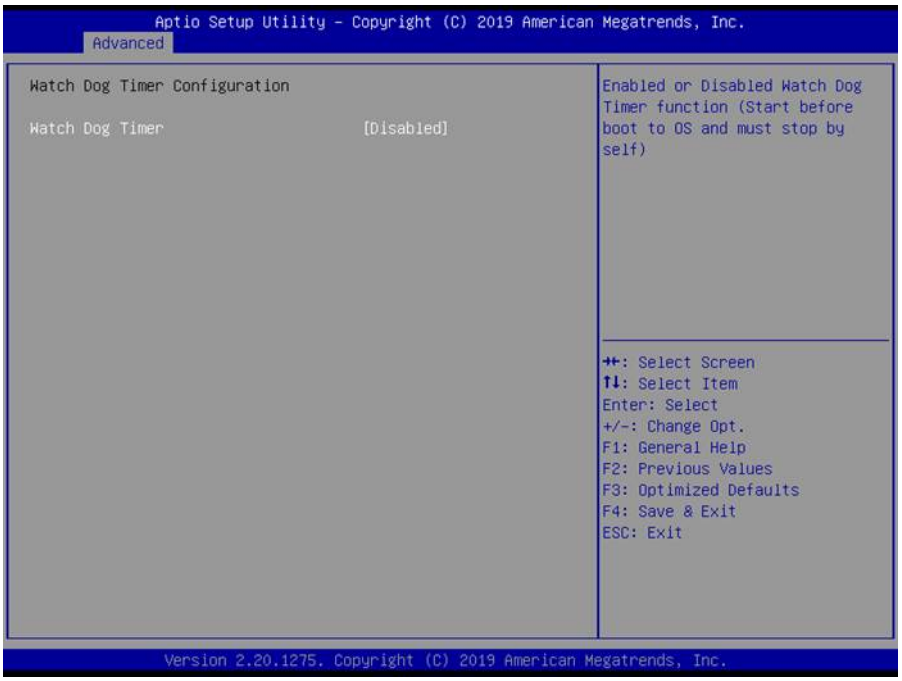



- **Serial Port**
  Enable or Disable Serial Port (COM).
- **Change Settings**
  Select an optimal settings for Super I/O device.
- **COM Port Mode**
  COM Port Mode Select.

### Hardware Monitor

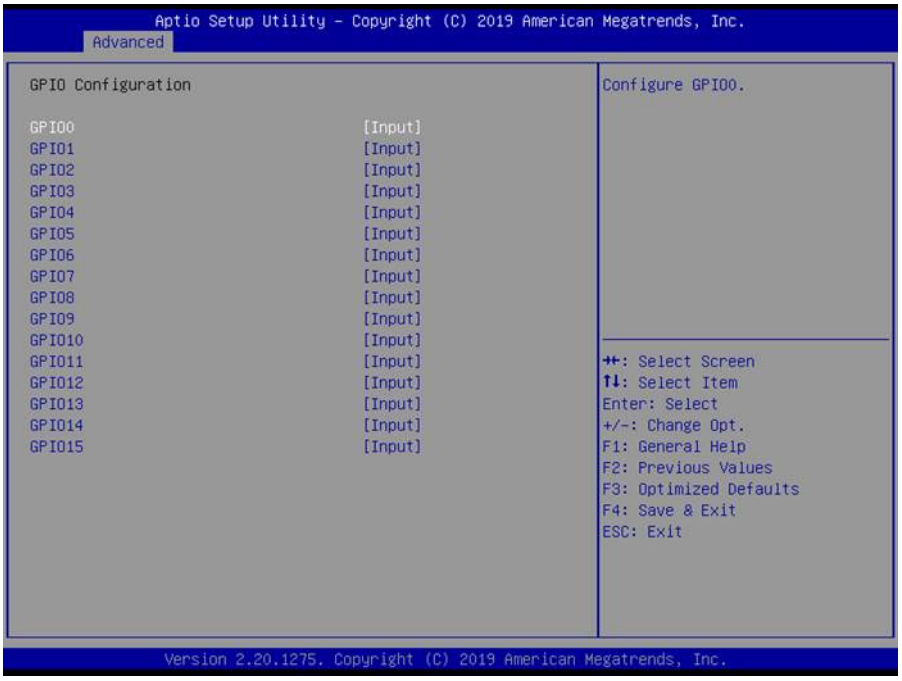


### Watchdog Timer Configuration




- **Watchdog Timer**
  Enable or Disable Watchdog Timer Function.

### GPIO Configuration




- **GPIO0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15**
  Configure GPIO 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15.

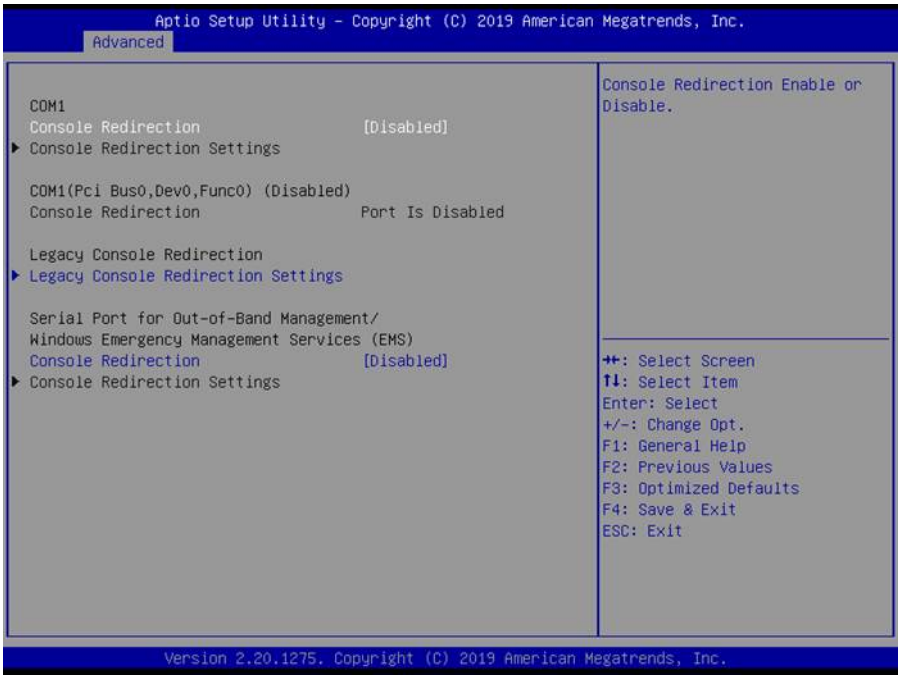
### 3.1.2.6 Trusted Computing


- **Security Device Support**
  Enable or disable BIOS support for security device.
- **SHA-1 PCR Bank**
  Enable or Disable SHA-1 PCR Bank.
- **SHA256 PCR Bank**
  Enable or Disable SHA256 PCR Bank.
- **Pending Operation**
  Schedule an Operation for the Security Device.
- **Platform Hierarchy**
  Enable or Disable Platform Hierarchy.
- **Storage Hierarchy**
  Enable or Disable Storage Hierarchy.
- **Endorsement Hierarchy**
  Enable or Disable Endorsement Hierarchy.
- **TPM 2.0 UEFI Spec Version**
  Select the TCG2 Spec Version Support.
- **Physical Presence Spec Version**
  Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3.
- **Device Select**
  TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices.

### 3.1.2.7 S5 RTC Wake Settings


- **Wake System from S5**
  Enable or disable System wake on alarm event. Select FixedTime, system will-wake on the hr::min::sec specified.

### 3.1.2.8 Serial Port Console Redirection

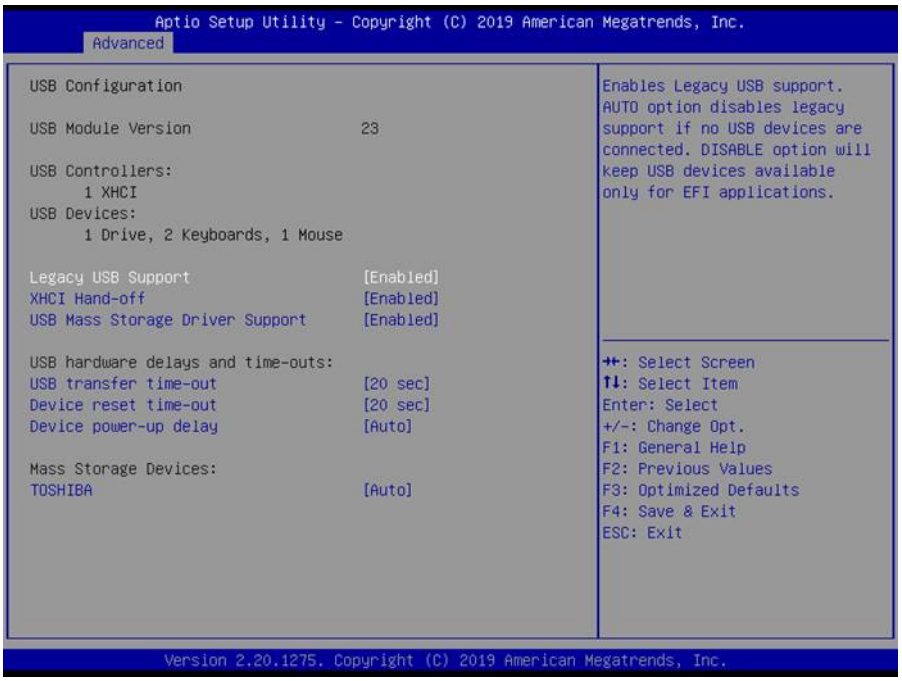



- **Console Redirection**
  This item allows users to enable or disable console redirection for Microsoft Windows Emergency Management Services (EMS).
- **Console Redirection**
  This item allows users to configuration console redirection detail settings.

### 3.1.2.9 Intel TXT Information

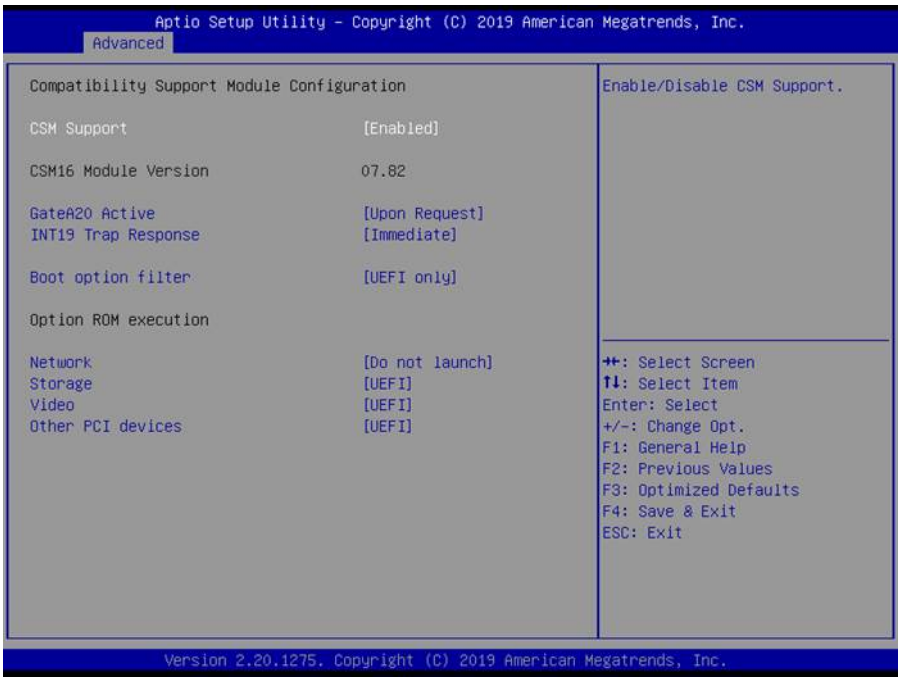

- **Intel TXT Information**
  Display Intel TXT information.

### 3.1.2.10 USB Configuration



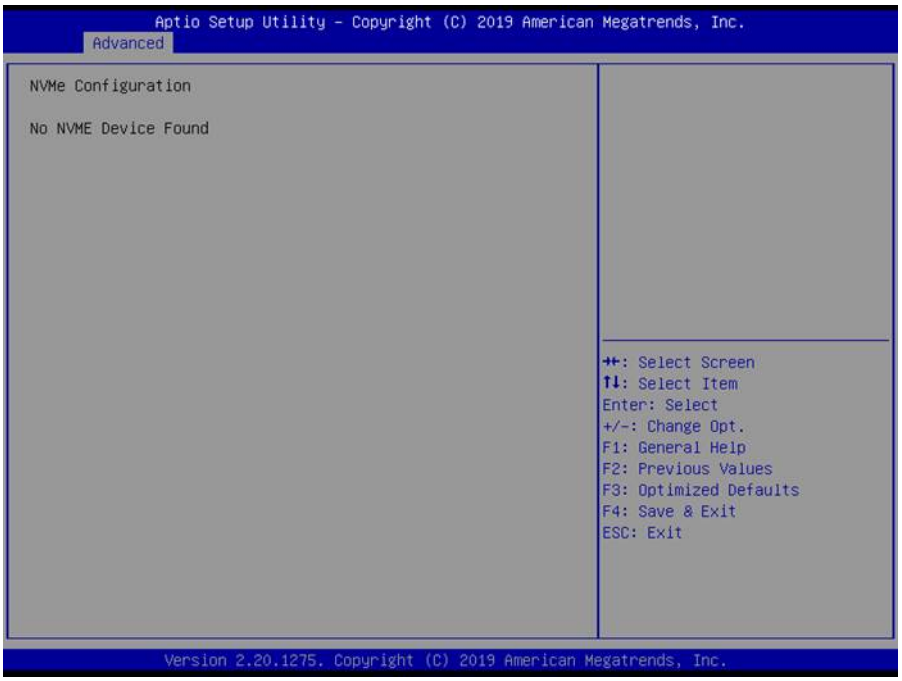

- **Legacy USB Support**
  Enables Legacy USB support. AUTO option disables legacy support if no US devices are connected. DISABLE option will keep USB devices available only for EFI applications.
- **XHCI Hand-Off**
  This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
- **USB Mass Storage Driver Support**
  Enable/Disable USB Mass Storage Driver Support.
- **USB Transfer Time-Out**
  Time-out value for control, Bulk, and interrupt transfers.
- **Device Reset Time-Out**
  USB mass storage device start unit command time-out.
- **Device Power-Up delay**
  Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.

### 3.1.2.11 CSM Configuration




- **CSM Support**
  Enable/Disable CSM Support.
- **GateA20 Active**
  UPON REQUEST - GA20 can be disabled using BIOS services. ALWAYS - do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.
- **Option ROM Message**
  BIOS Set display mode for Option ROM.
- **INT19 Trap Response**
  BIOS reaction on INT19 trapping by Option ROM: IMMEDIATE - execute the trap right away; POSTPONED - execute the trap during legacy boot.
- **Boot Option Filter**
  This option controls Legacy/UEFI ROMs priority.
- **Network**
  Controls the execution of UEFI and Legacy PXE OpROM.
- **Storage**
  Controls the execution of UEFI and Legacy Storage OpROM.
- **Video**
  Controls the execution of UEFI and Legacy Video OpROM.
- **Other PCI devices**
  Determines OpROM execution policy for devices other than Network, Storage, or Video.

### 3.1.2.12 NVMe Configuration




### 3.1.2.13 SDIO Configuration


- **SDIO Access Mode**
  Select access SD device in DMA mode or PIO mode.

#### 3.1.2.14 Network Stack Configuration


- **Network Stack**
  Enable/Disable UEFI Network Stack.

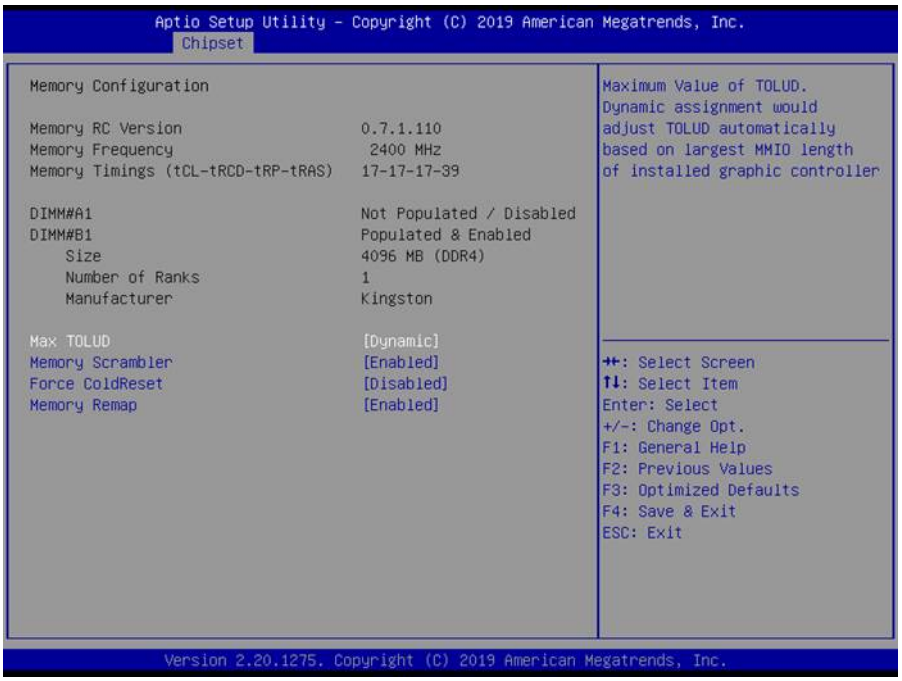
### 3.1.3 Chipset Configuration

Select the Chipset tab from the MIO-5373 setup screen to enter the Chipset BIOS Setup screen. You can display a Chipset BIOS Setup option by highlighting it using the <Arrow> keys. All Plug and Play BIOS Setup options are described in this section. The Plug and Play BIOS Setup screen is shown below.

### 3.1.3.1 System Agent (SA) Configuration

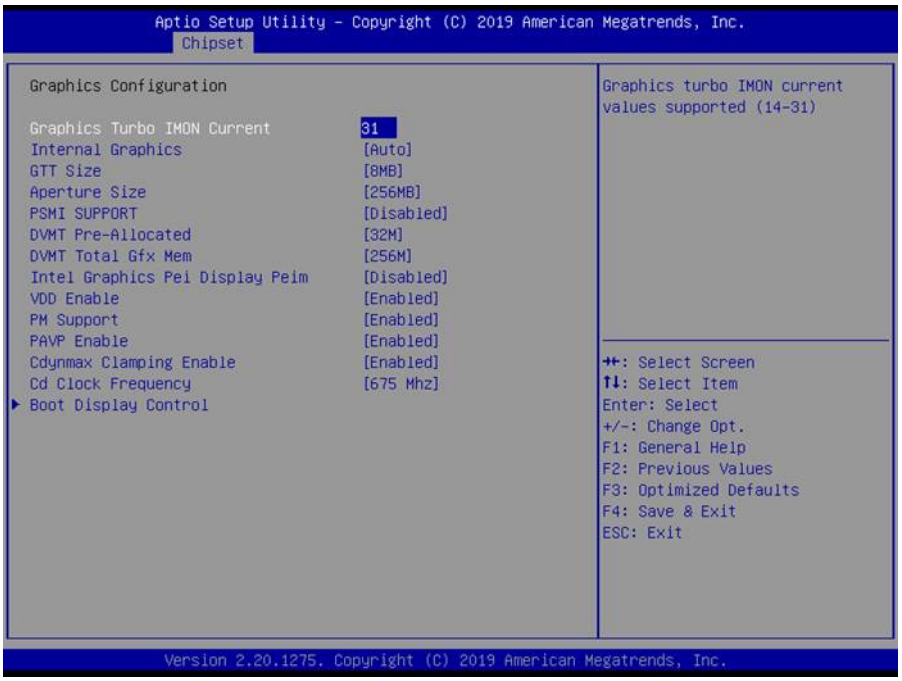

- **Memory Configuration**
  Memory Configuration Parameters.
- **Graphics Configuration**
  Graphics Configuration Parameters.
- **VT-d**
  VT-D capability.
- **Above 4GB MMIO BIOS Assignment**
  Enable/Disable above 4GB Memory Mapped IO BIOS assignment.
- **X2APIC Opt Out**
  Enable/Disable X2APIC Opt Out Bit.

### Memory Configuration



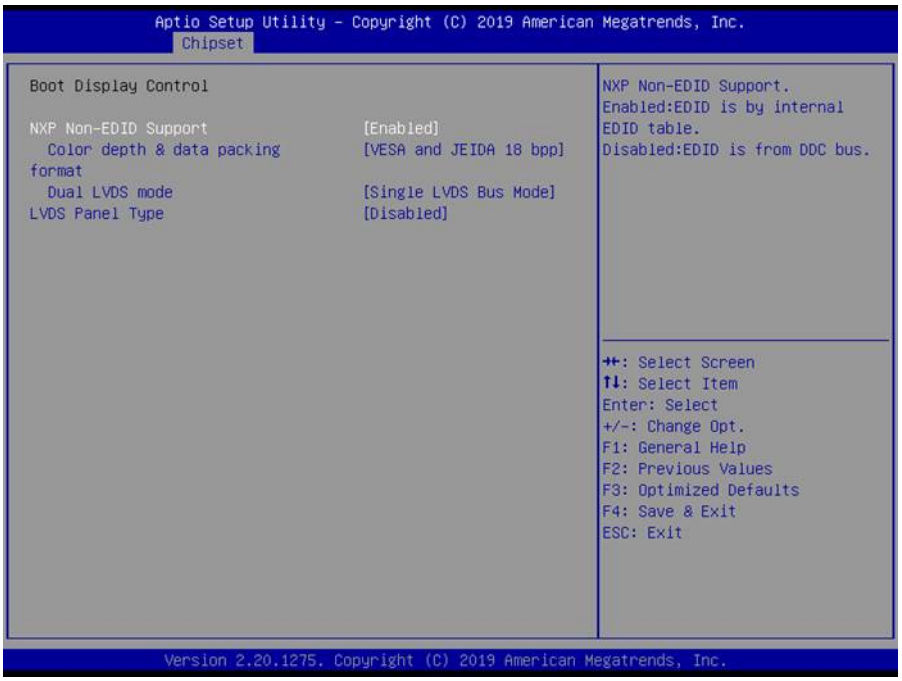

- **Max TOLUD**
  Maximum Value of TOLUD.
- **Memory Scrambler**
  Enable/Disable Memory Scrambler support.
- **Force ColdReset**
  Force ColdReset OR Choose MrcColdBoot mode.
- **Memory Remap**
  Enable/Disable Memory Remap above 4GB.

### Graphics Configuration



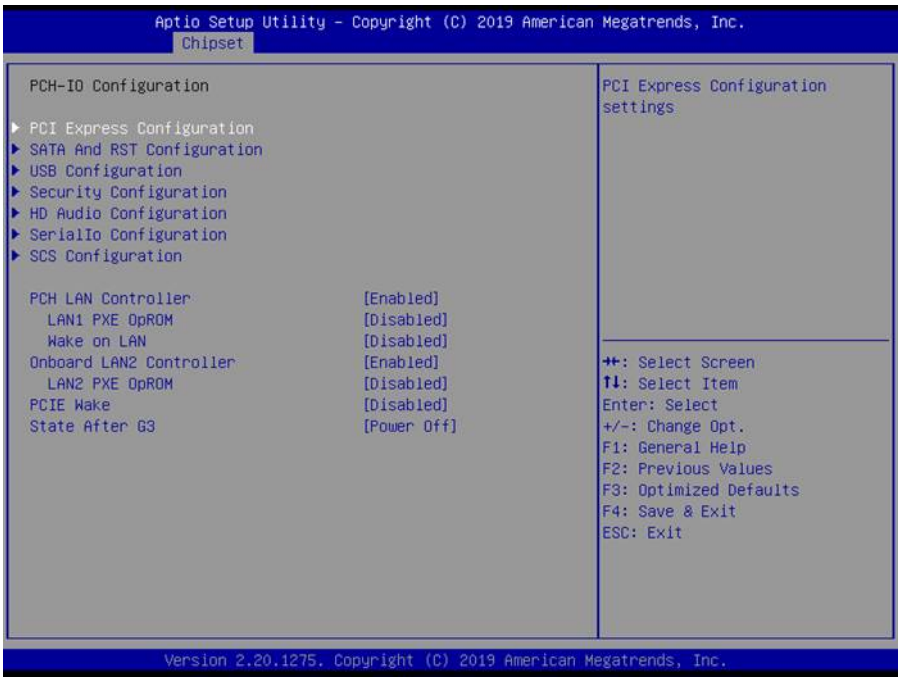

- **Graphics Turbo IMON Current**
  Graphics turbo IMON current values supported.
- **Internal Graphics**
  Keep IGFX enabled based on the setup options.
- **GTT Size**
  Select the GTT Size.
- **Aperture Size**
  Select the Aperture Size.
- **DVMT Pre-Allocated**
  Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
- **DVMT Total Gfx Mem**
  Select DVMT 5.0 Total Graphic Memory size used by the Internal Graphics Device.
- **Gfx Low Power Mode**
  This option is applicable for SFF only.
- **PM Support**
  Enable/Disable PM Spport.
- **PAVP Enable**
  Enable/Disable PAVP.
- **CD Clock Frequency**
  Select the highest Cd clock frequency supported by this platform.

### Boot Display Control



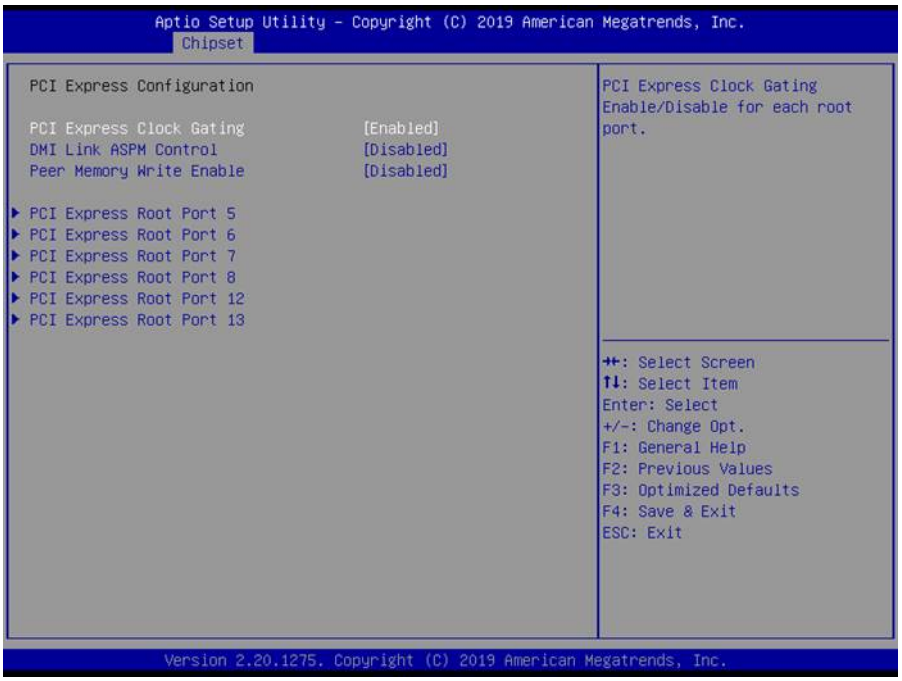

- **NXP Non-EDID Support**
  NXP Non-EDID Support.
- **Color Depth & Data Packing**
  Color depth and data packing format for Non-EDID Support.
- **Dual LVDS Mode**
  Select LVDS bus to Single bus mode or Dual bus mode.
- **LVDS Panel Type**
  This item allow user to select LVDS panel type.

### 3.1.3.2 PCH-IO Configuration



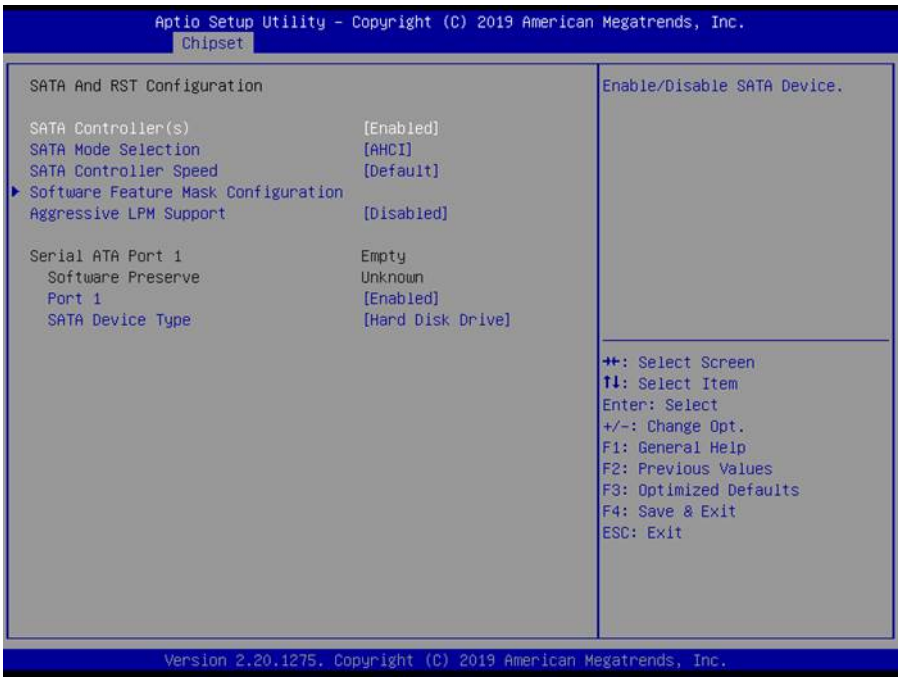

- **PCI Express Configuration**
  PCI Express Configuration Settings.
- **SATA And RST Configuration**
  SATA Device Options Settings.
- **USB Configuration**
  USB Configuration Settings.
- **Security Configuration**
  Security Configuration Settings.
- **HD Audio Configuration**
  HD Audio Subsystem Configuration Settings.
- **SerialIO Configuration**
  SerialIO Configuration Settings.
- **SCS Configuration**
  Storage and Communication Subsystem Configuration.
- **PCH LAN Controller**
  Enable or Disable onboard NIC.
- **LAN1 PXE ROM**
  Enable or Disable onboard LAN's PXE option ROM.
- **Wake on LAN**
  Enable or Disable Integrated LAN to wake the system from S5.
- **Onboard LAN2 Controller**
  Enable or Disable onboard NIC.
- **LAN2 PXE ROM**
  Enable or Disable onboard LAN's PXE option ROM.
- **PCIE Wake**
  Enable or Disable PCIE to wake the system from S5.
- **State After S3**
  Specify what state to go to when power is re-applied after a power failure (G3 state).

### PCI Express Configuration




- **PCI Express Root Port 5/6/7/8/12/13**
  PCI Express Port 5/6/7/8/12/13 Settings.

### SATA and RST Configuration




- **SATA Controller(s)**
  Enable/Disable SATA Device.
- **SATA Mode Selection**
  Determine how SATA controller operates.
- **SATA Controller Speed**
  Indicates the maximum speed the SATA controller can support.
- **Software Feature Mask Configuration**
  RST Legacy ROM/RST UEFI Driver will refer to the SWFM configuration to enable/disable the storage feature.
- **Aggressive LPM Support**
  Enabled PCH to aggressively enter link power state.

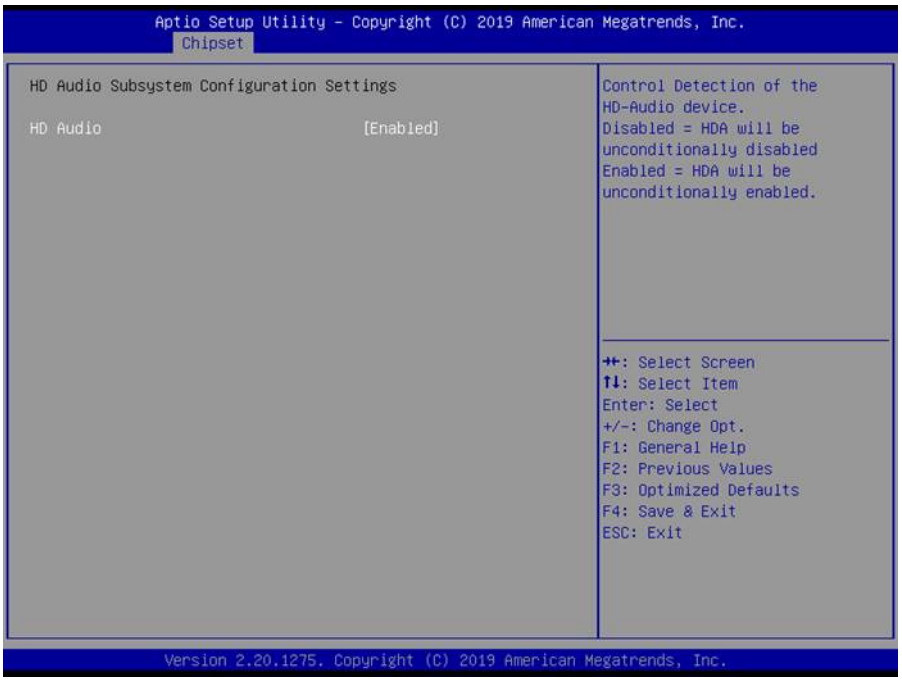
### USB Configuration


- **XHCI Disable Compliance Mode**
  Option to disable Compliance Mode.
- **USB Port Disable Override**
  Selectively Enable/Disable the corresponding USB Port from reporting a Device Connection to the Controller.

### Security Configuration


- **RTC Lock**
  Enable will lock bytes 38h-3Fh in the lower/upper 128-byte bank of RTC RAM.
- **BIOS Lock**
  Enable or Disable the PCH BIOS Lock Enable feature.

### HD Audio Configuration

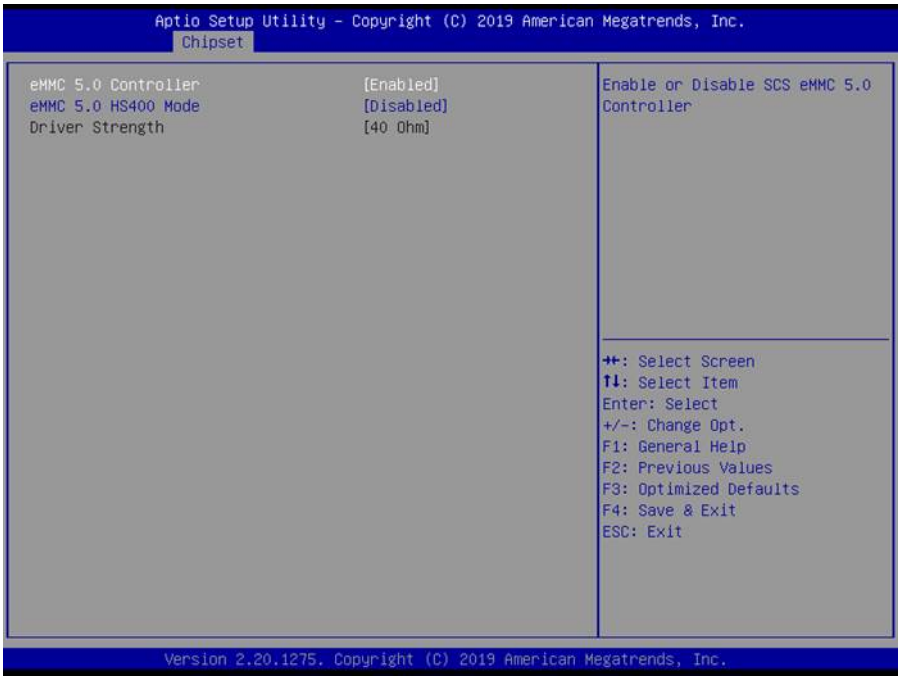



- **HD Audio**
  Control Detection of the HD-Audio device. Disabled = HDA will be uncondition-ally disabled. Enabled = HDA will be unconditionally Enabled.

### Serial I/O Configuration

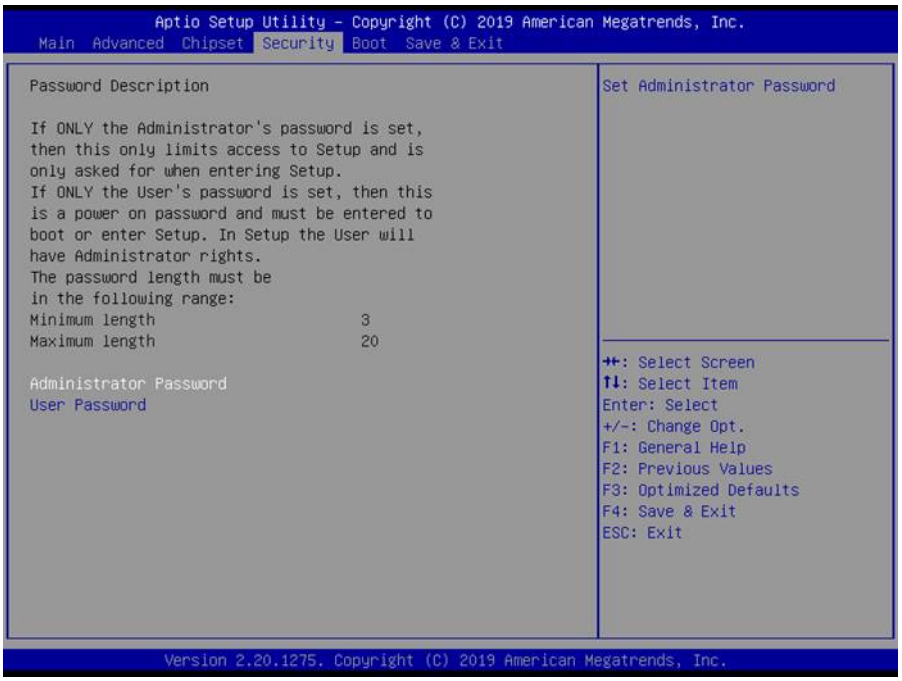

- **I2C0 Controller**
  Enable/Disables Serial I/O Controller.

### SCS Configuration




- **eMMC 5.0 Controller**
  Enable or Disable SCS eMMC 5.0 Controller.

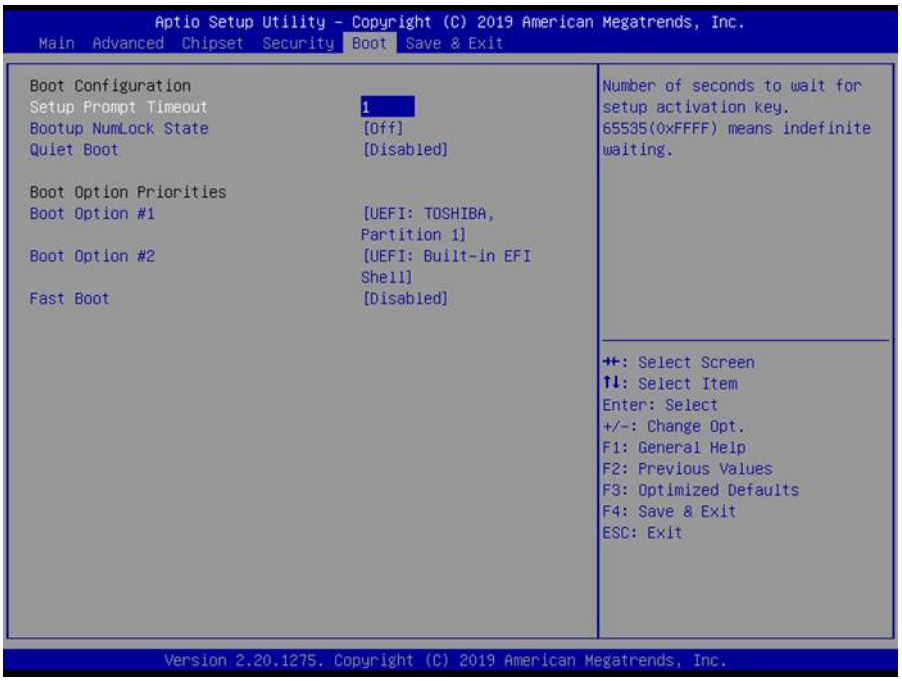
### 3.1.4 Security




Select Security Setup from the MIO-5373 Setup main BIOS setup menu. All Security Setup options, such as password protection and virus protection are described in this section. To access the sub menu for the following items, select the item and press <Enter>:

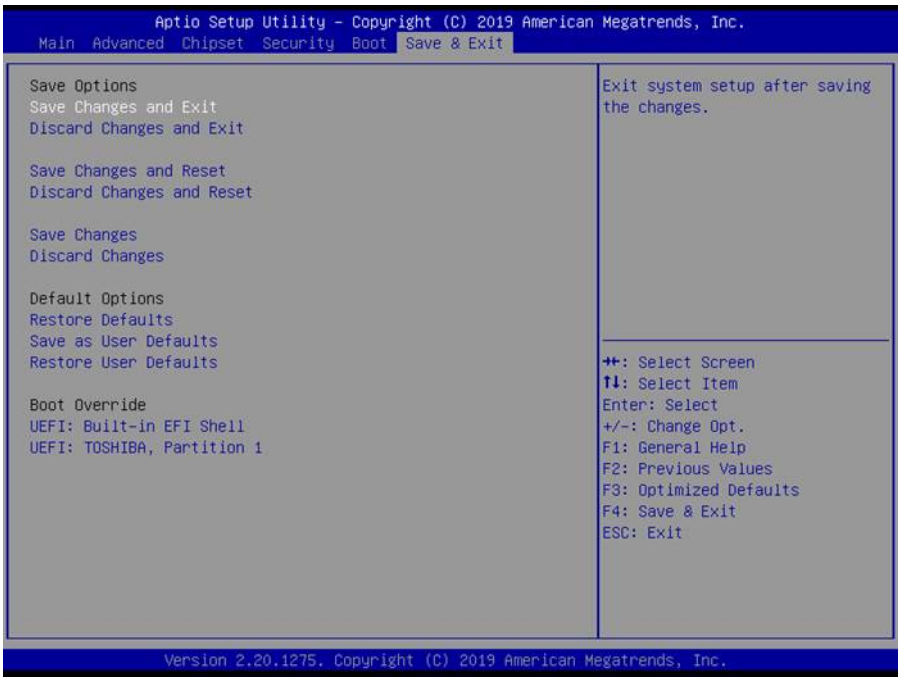
- **Change Administrator / User Password**
  Select this option and press <ENTER> to access the sub menu, and then type in the password.

### 3.1.5 Boot




- **Setup Prompt Timeout**
  Number of seconds that the firmware will wait before initiating the original default boot selection. A value of 0 indicates that the default boot selection is to be initiated immediately on boot. A value of 65535(0xFFFF) indicates that firmware will wait for user input before booting. This means the default boot selection is not automatically started by the firmware.
- **Bootup NumLock State**
  Select the keyboard NumLock state.
- **Quiet Boot**
  Enables or disables Quiet Boot option.
- **Boot Option #1**
  Sets the system boot order.
- **Fast Boot**
  Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

### 3.1.6 Save & Exit




- **Save Changes and Exit**
  This item allows you to exit system setup after saving the changes.
- **Discard Changes and Exit**
  This item allows you to exit system setup without saving any changes.
- **Save Changes and Reset**
  This item allows you to reset the system after saving the changes.
- **Discard Changes and Reset**
  This item allows you to rest system setup without saving any changes.
- **Save Changes**
  This item allows you to save changes done so far to any of the options.
- **Discard Changes**
  This item allows you to discard changes done so far to any of the options.
- **Restore Defaults**
  This item allows you to restore/load default values for all the options.
- **Save as User Defaults**
  This item allows you to save the changes done so far as user defaults.
- **Restore User Defaults**
  This item allows you to restore the user defaults to all the options.
- **Boot Override**
  Boot device select can override your boot priority.

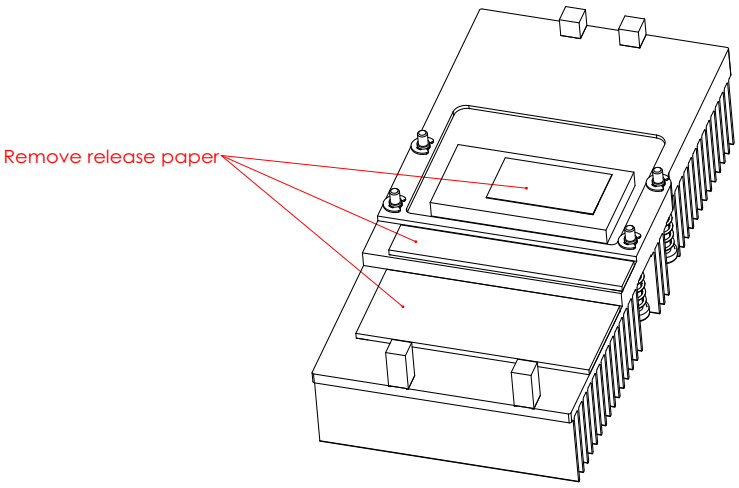
# Chapter 4

## MIOe Installation

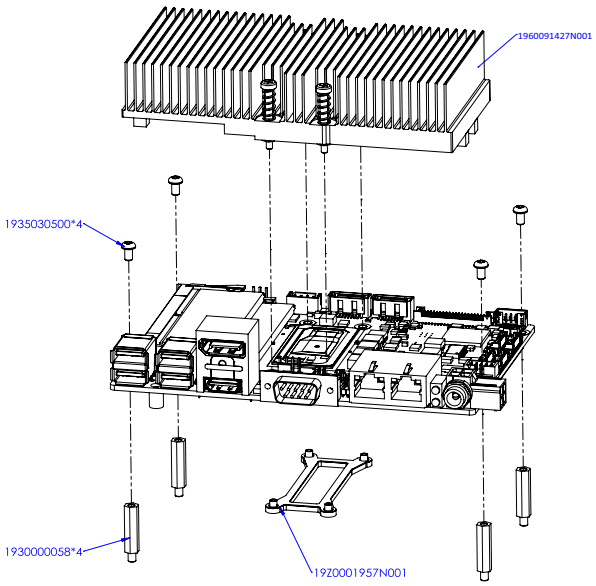
The MI/O compact form factor SBC is a next-generation SBC with a variety of mechanical improvements. The following is a quick installation guide for our thermal design and MIOe module.

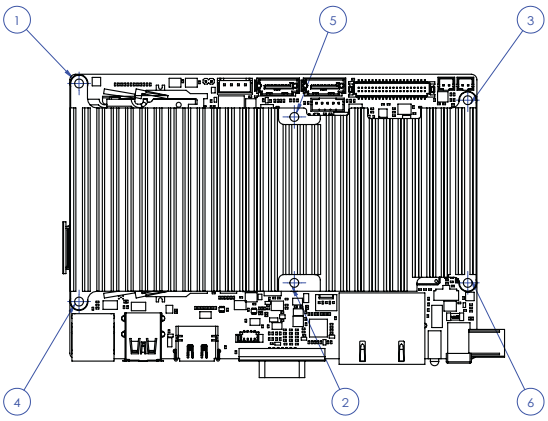
## 4.1 Quick Installation Guide

1. There is a heatsink/cooler in the white box inside the package. Carefully remove the release paper from the thermal pad before installation.




2. There are four screws inside the white box, please install the heatsink into place and follow assembly sequence below:




1
5
3
4
2
6

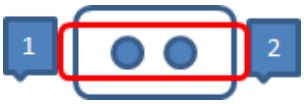
# Appendix A

## Pin Assignments

**This appendix contains detailed/ specialized information.**

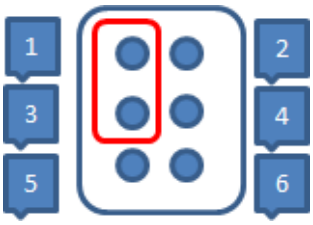
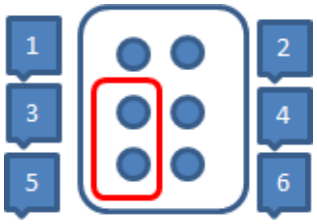
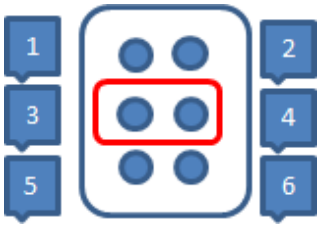
# A.1 Jumper Settings

## A.1.1 J1: ATX/AT Mode Selection

| Function | Jumper Setting |
|---|---|
| AT Mode (Default) |  |
| ATX Mode |  |

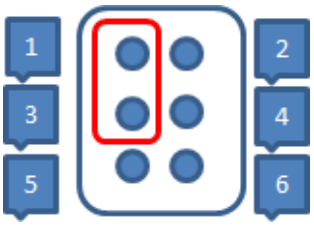
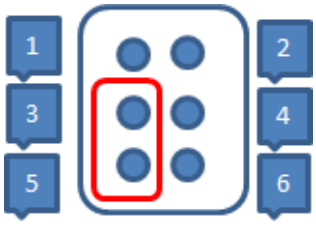
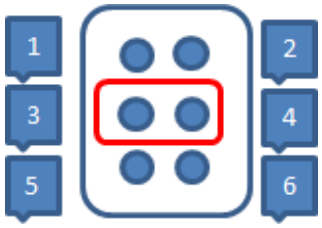
| Pin | Signal Pin Definition |
|---|---|
| 1 | AT_DET# |
| 2 | GND |

## A.1.2 J2: RI# 5V/12V Selection Pin for CN9

| Function | Jumper Setting |
|---|---|
| RI# Voltage Setting: +V5 |  |
| RI# Voltage Setting: +V12 |  |
| RI# Voltage Setting: RI# (Default) |  |

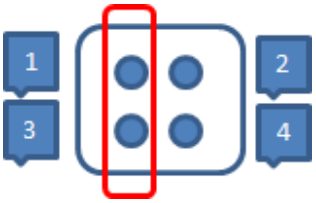
| Pin | Signal Pin Definition |
|---|---|
| 1 | +V5 |
| 2 | CN9_RI# |
| 3 | COM_RI# |
| 4 | CN9_RI# |
| 5 | +V12 |
| 6 | CN9_RI# |

### A.1.3 J3: Panel Voltage Selection

| Function | Jumper Setting |
|---|---|
| Panel Voltage Setting: +V3.3(Default) |  |
| Panel Voltage Setting: +V5 |  |
| Panel Voltage Setting: +V12 |  |

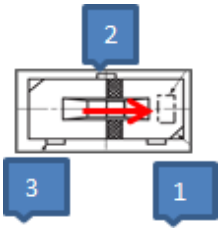
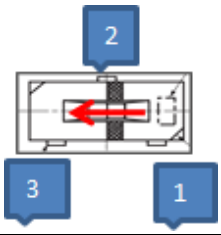
| Pin | Signal Pin Definition |
|---|---|
| 1 | +V3.3 |
| 2 | NC |
| 3 | +V_CH7511B_LCD |
| 4 | +V12 |
| 5 | +V5 |
| 6 | NC |

### A.1.4 J4: JEIDA and VESA Mode Selection

| Function | Jumper Setting |
|---|---|
| JEIDA Mode Setting: +V3.3 |  |
| VESA Mode Setting: GND (Default) |  |

| Pin | Signal Pin Definition |
|---|---|
| 1 | LVDS1_VCON |
| 2 | LVDS1_VCC |
| 3 | GND |
| 4 | NC |

### A.1.5 SW1: Clear CMOS

| Function | Jumper Setting |
|---|---|
| Keep COMS Data (Default) |  |
| Clear CMOS Date |  |

| Pin | Signal Pin Definition |
|---|---|
| 1 | RTC_a_RST# |
| 2 | RTC_RST# |
| 3 | GND |

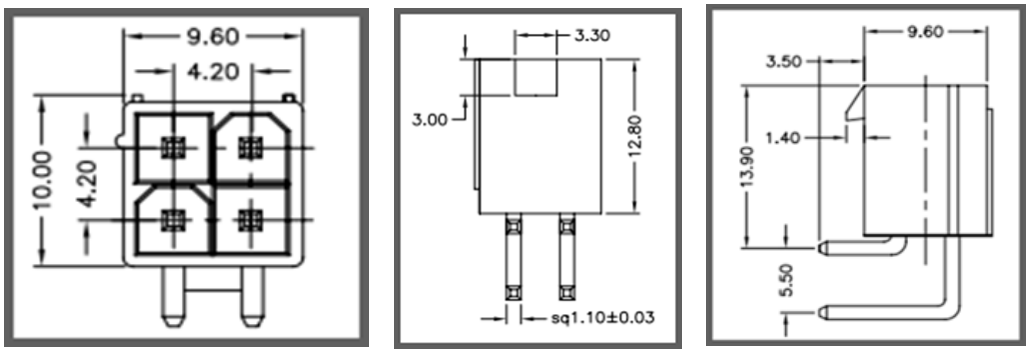
## A.2 Connector and Header List

**Table A.1: Connector and Header List:**

| | Description | Location Name |
|---|---|---|
| 1 | DDR4 SODIMM 260P/H5.2mm | CN1 |
| 2 | DDR4 SODIMM 260P/H9.2mm | CN2 |
| 3 | DC Input Connector | CN3 |
| 4 | RTC Battery Connector | CN5 |
| 5 | Power/LED/Case Open/Buzzer Connector | CN8 |
| 6 | COM Port Connector (RS232+RS422+RS485) | CN9 |
| 7 | COM Port Connector (RS232+RS422+RS485) | CN10 |
| 8 | RJ45 Connector (2 port) | CN11 |
| 9 | Inverter Connector | CN12 |
| 10 | LVDS Connector | CN13 |
| 11 | eDP Connector | CN14 |
| 12 | HDMI and DP++ Connector | CN15 |
| 13 | Key E Connector | CN16 |
| 14 | Key B and Key M (option) Connector | CN17 |
| 15 | SIM Card Connector | CN20 |
| 16 | USB 3.1 Connector (2 ports) | CN22 |
| 17 | USB 3.1 Connector (2 ports) | CN23 |
| 18 | Internal USB Connector | CN24 |
| 19 | HDD Power Connector | CN25 |
| 20 | HDD Connector | CN26 |
| 21 | HDD Connector | CN27 |
| 22 | GPIO/RS232 Connector | CN28 |
| 23 | Audio Connector | CN29 |
| 24 | GPIO/RS232 Connector | CN30 |
| 25 | MIOe Connector | CN30A1 |
| 26 | I2C Bus Connector | CN31 |
| 27 | System FAN Connector | CN32 |
| 28 | CANBus Connector | CN35 |
| 29 | SMBus Connector | CN36 |
| 30 | DC input Connector (Adapter) | CN37 |

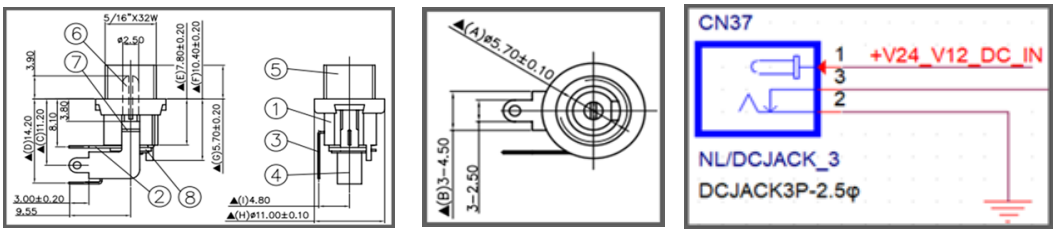
# A.3 Connector and Header List Description

## A.3.1 DC Input Connector



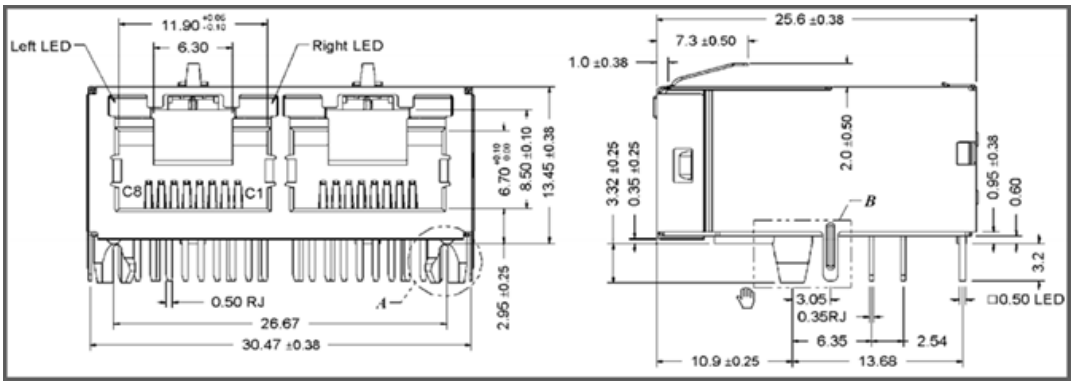

| Pin | Signal Pin Definition |
|---|---|
| 1 | GND |
| 2 | GND |
| 3 | +V24_V12_DC_IN |
| 4 | +V24_V12_DC_IN |

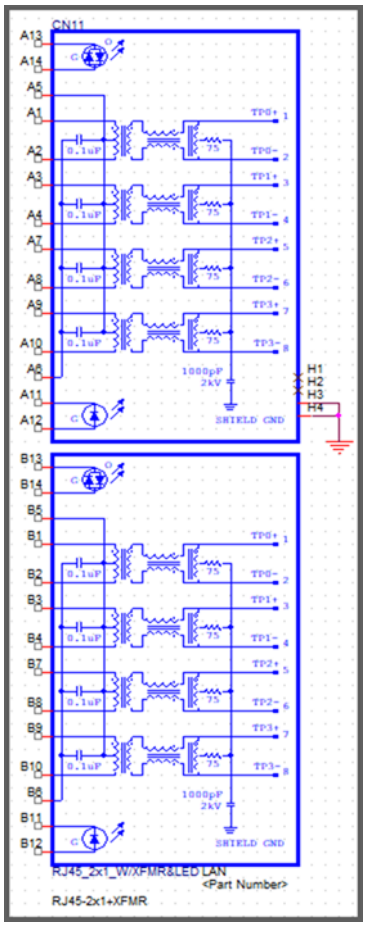
## A.3.2 DC Input Connector (Adapter)




| Pin | Signal Pin Definition |
|---|---|
| 1 | +V24_V12_DC_IN |
| 2 | NC |
| 3 | GND |

## A.3.3 RJ45 (2 Ports)

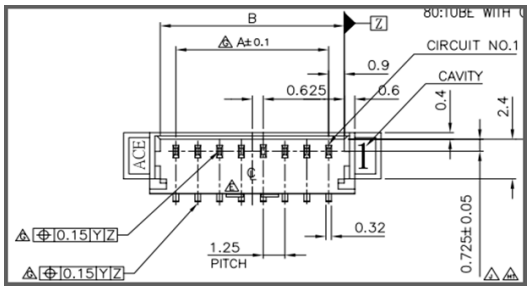


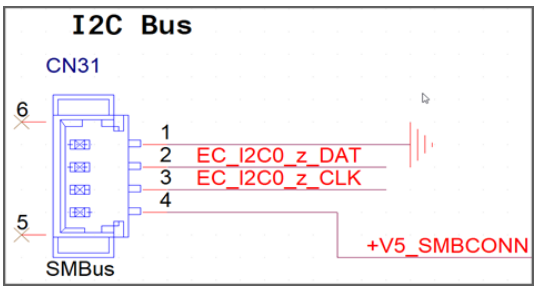




| Pin | Signal Pin Definition |
|---|---|
| A1 | LAN1_MDIO+ |
| A2 | LAN1_MDIO- |
| A3 | LAN1_MDI1+ |
| A4 | LAN1_MDI1- |
| A5 | LAN1CONN |
| A6 | LAN1_GND |
| A7 | LAN1_MDI2+ |
| A8 | LAN1_MDI2- |
| A9 | LAN1 MDI3+ |

| | |
|---|---|
| A10 | LAN1_MDI3- |
| A11 | LAN1_ACT# |
| A12 | LAN1_A_ACT# |
| A13 | LAN1_A_LINK100# |
| A14 | LAN1_A_LINK1000# |
| B1 | LAN2_MDIO+ |
| B2 | LAN2_MDIO- |
| B3 | LAN2_MDI1+ |
| B4 | LAN2_MDI1- |
| B5 | LAN2CONN |
| B6 | LAN2_GND |
| B7 | LAN2_MDI2+ |
| B8 | LAN2_MDI2- |
| B9 | LAN2_MDI3+ |
| B10 | LAN2_MDI3- |
| B11 | LAN2_ACT# |
| B12 | LAN2_A_ACT# |
| B13 | LAN2_A_LINK100# |
| B14 | LAN2_A_LINK1000# |

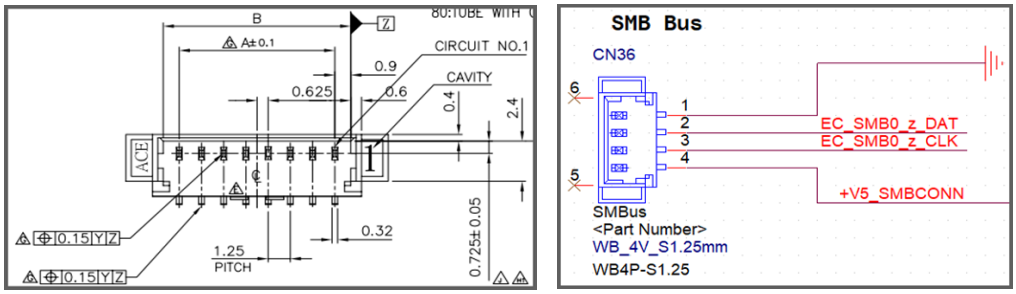
## A.3.4 I2C Bus Connector



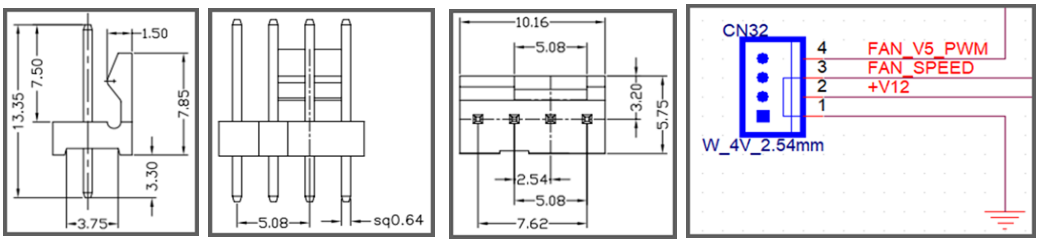

| Pin | Signal Pin Definition |
|---|---|
| 1 | GND |
| 2 | I2C_DAT |
| 3 | I2C_CLK |
| 4 | +V5 |

## A.3.5 SMBus Connector



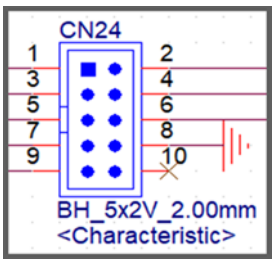

| Pin | Signal Pin Definition |
|---|---|
| 1 | GND |
| 2 | SMBus_DAT |
| 3 | SMBus_CLK |
| 4 | +V5 |

## A.3.6 System FAN Connector



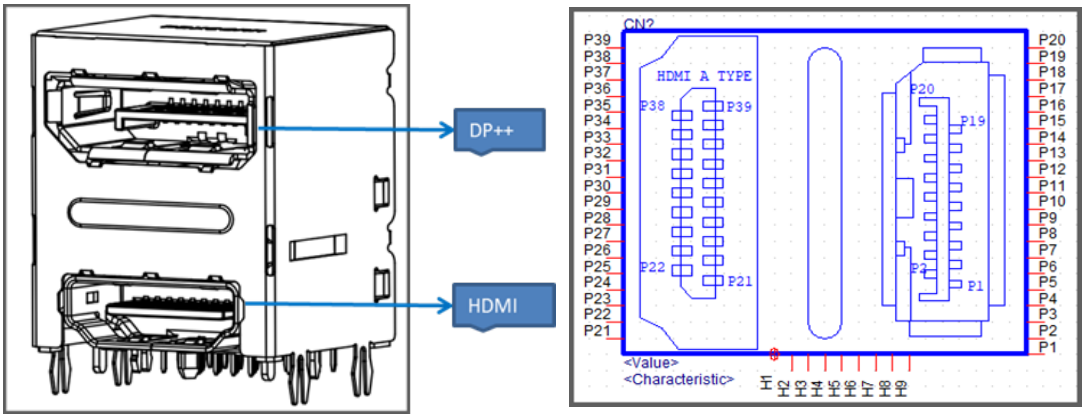

| Pin | Signal Pin Definition |
|---|---|
| 1 | GND |
| 2 | +12V |
| 3 | FAN_SPEED |
| 4 | FAN_PWM |

## A.3.7 Internal USB Connector



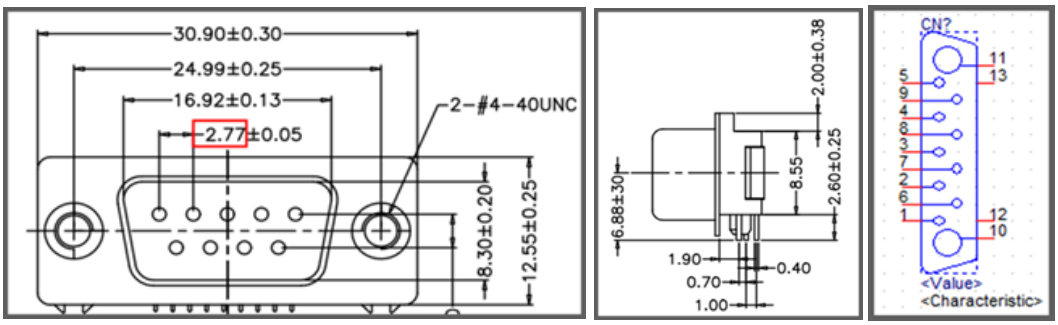

| Pin | Signal Pin Definition |
|---|---|
| 1 | +V5SB |
| 2 | +V5SB |
| 3 | USB8_P- |
| 4 | USB9_P- |
| 5 | USB8_P+ |
| 6 | USB9_P+ |
| 7 | GND |
| 8 | GND |
| 9 | GND |
| 10 | NC |

## A.3.8 HDMI and DP++ Connector



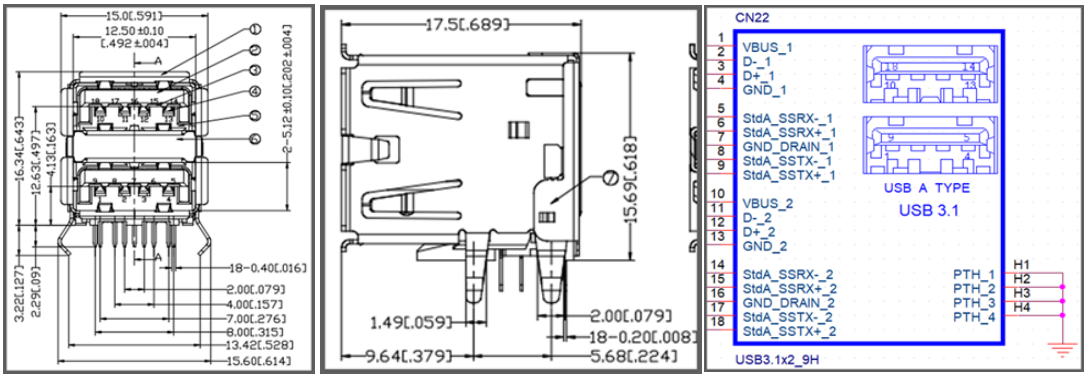

| Pin | Signal Pin Definition | Pin | Signal Pin Definition |
|---|---|---|---|
| P21 | HDMI1_Z_TX2+ | P1 | DP_TX0+ |
| P22 | GND | P2 | GND |
| P23 | HDMI1_Z_TX2- | P3 | DP_TX0- |
| P24 | HDMI1_Z_TX1+ | P4 | DP_TX1+ |
| P25 | GND | P5 | GND |
| P26 | HDMI1_Z_TX1- | P6 | DP_TX1- |
| P27 | HDMI1_Z_TX0+ | P7 | DP_TX2+ |
| P28 | GND | P8 | GND |
| P29 | HDMI1_Z_TX0- | P9 | DP_TX2- |
| P30 | HDMI1_Z_DCLK+ | P10 | DP_TX3+ |
| P31 | GND | P11 | GND |
| P32 | HDMI1_Z_DCLK- | P12 | DP_TX3- |
| P33 | NC | P13 | DP_AUX_EN# |
| P34 | NC | P14 | GND |
| P35 | HDMI1_SCL | P15 | DP_AUX+ |
| P36 | HDMI1_SDA | P16 | GND |
| P37 | GND | P17 | DP1_AUX- |
| P38 | +V5_HDMI1 | P18 | DDP2_DP_HPD |
| P39 | DDP1_HDMI_HPD | P19 | GND |
| | | P20 | +V3.3_DP |

## A.3.9 COM Port Connector (RS232+RS422+RS485)



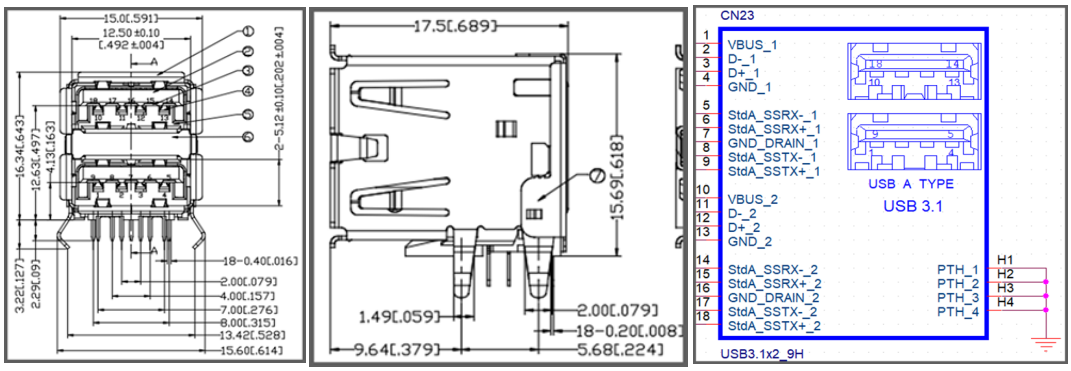

| Pin | Signal Pin Definition |
|---|---|
| 1 | 422TX-/485D-/DCD# |
| 2 | 422TX+/485D+/RXD |
| 3 | 422RX+/TXD |
| 4 | 422RX-/DTR# |
| 5 | GND |
| 6 | DSR# |
| 7 | RTS# |
| 8 | CTS# |
| 9 | RI# |

## A.3.10 USB 3.1 Connector (2 Ports)



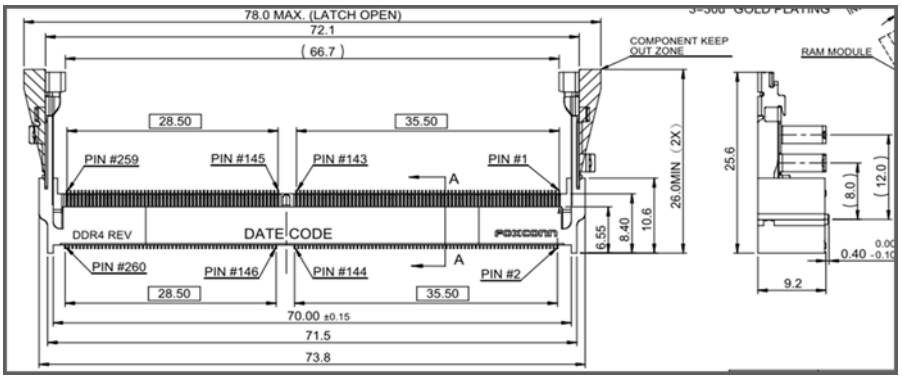

| Pin | Signal Pin Definition |
|---|---|
| 1 | +V5 |
| 2 | USB1_P- |
| 3 | USB1_P+ |
| 4 | GND |
| 5 | USB1_SSRX- |
| 6 | USB1_SSRX+ |
| 7 | GND |
| 8 | USB1_SSTX- |
| 9 | USB1_SSTX+ |
| 10 | +V5 |
| 11 | USB2_P- |
| 12 | USB2_P+ |
| 13 | GND |
| 14 | USB2_SSRX- |
| 15 | USB2_SSRX+ |
| 16 | GND |
| 17 | USB2_SSTX- |
| 18 | USB2_SSTX+ |
| H1 | GND |
| H2 | GND |
| H3 | GND |
| H4 | GND |

## A.3.11 USB3.1 Connector (2 Ports)




| Pin | Signal Pin Definition |
|---|---|
| 1 | +V5 |
| 2 | USB3_P- |
| 3 | USB3_P+ |
| 4 | GND |
| 5 | USB3_SSRX- |
| 6 | USB3_SSRX+ |
| 7 | GND |
| 8 | USB3_SSTX- |
| 9 | USB3_SSTX+ |
| 10 | +V5 |
| 11 | USB4_P- |
| 12 | USB4_P+ |
| 13 | GND |
| 14 | USB4_SSRX- |
| 15 | USB4_SSRX+ |
| 16 | GND |
| 17 | USB4_SSTX- |
| 18 | USB4_SSTX+ |
| H1 | GND |
| H2 | GND |
| H3 | GND |
| H4 | GND |

## A.3.12 DDR4 SODIMM 260P/H9.2mm




| Pin | Signal Pin Definition |
|---|---|
| 1 | GND |
| 2 | GND |
| 3 | MB_MD8 |
| 4 | MB_MD11 |
| 5 | GND |
| 6 | GND |
| 7 | MB_MD15 |
| 8 | MB_MD14 |
| 9 | GND |
| 10 | GND |
| 11 | MB_DQS1- |
| 12 | +V1.2DDR |
| 13 | MB_DQS1+ |
| 14 | GND |
| 15 | GND |
| 16 | MB_MD12 |
| 17 | MB_MD13 |
| 18 | GND |
| 19 | GND |
| 20 | MB_MD9 |
| 21 | MB_MD10 |
| 22 | GND |
| 23 | GND |
| 24 | MB_MD2 |
| 25 | MB MD3 |
| 26 | GND |
| 27 | GND |
| 28 | MB_MD7 |
| 29 | MB_MD0 |
| 30 | GND |
| 31 | GND |
| 32 | MB_DQS0- |
| 33 | +V1.2DDR |
| 34 | MB_DQS0+ |

| | |
|---|---|
| 35 | GND |
| 36 | GND |
| 37 | MB_MD1 |
| 38 | MB_MD4 |
| 39 | GND |
| 40 | GND |
| 41 | MB_MD6 |
| 42 | MB_MD5 |
| 43 | GND |
| 44 | GND |
| 45 | MB_MD21 |
| 46 | MB_MD17 |
| 47 | GND |
| 48 | GND |
| 49 | MB_MD20 |
| 50 | MB_MD16 |
| 51 | GND |
| 52 | GND |
| 53 | MB_DQS2- |
| 54 | +V1.2DDR |
| 55 | MB_DQS2+ |
| 56 | GND |
| 57 | GND |
| 58 | MB_MD23 |
| 59 | MB_MD18 |
| 60 | GND |
| 61 | GND |
| 62 | MB_MD22 |
| 63 | MB_MD19 |
| 64 | GND |
| 65 | GND |
| 66 | MB_MD28 |
| 67 | MB_MD29 |
| 68 | GND |
| 69 | GND |
| 70 | MB_MD25 |
| 71 | MB_MD24 |
| 72 | GND |
| 73 | GND |
| 74 | MB_DQS3- |
| 75 | +V1.2DDR |
| 76 | MB_DQS3+ |
| 77 | GND |
| 78 | GND |
| 79 | MB_MD30 |
| 80 | MB_MD26 |
| 81 | GND |
| 82 | GND |

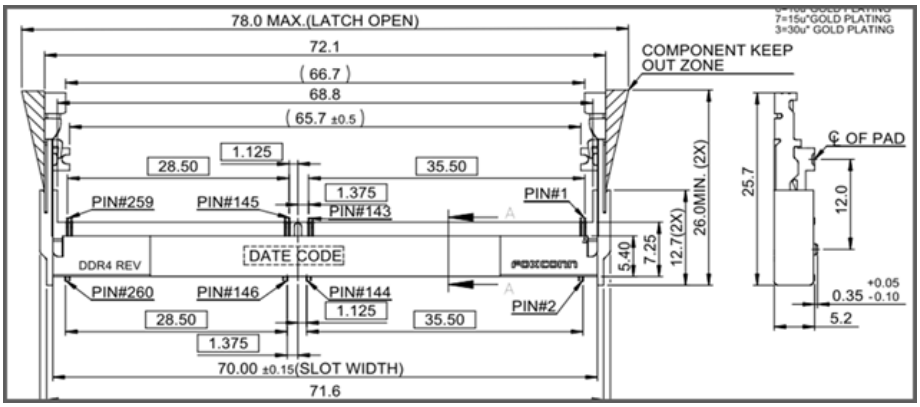
| | |
|---|---|
| 83 | MB_MD31 |
| 84 | MB_MD27 |
| 85 | GND |
| 86 | GND |
| 87 | MB_CB5 |
| 88 | MB_CB4 |
| 89 | GND |
| 90 | GND |
| 91 | MB_CB1 |
| 92 | MB_CB0 |
| 93 | GND |
| 94 | GND |
| 95 | MB_DQS8- |
| 96 | +V1.2DDR |
| 97 | MB_DQS8+ |
| 98 | GND |
| 99 | GND |
| 100 | MB_CB6 |
| 101 | MB_CB2 |
| 102 | GND |
| 103 | GND |
| 104 | MB_CB7 |
| 105 | MB_CB3 |
| 106 | GND |
| 107 | GND |
| 108 | DDR4_DRAMRST# |
| 109 | MB_CKE0 |
| 110 | MB_CKE1 |
| 111 | +V1.2DDR |
| 112 | +V1.2DDR |
| 113 | MB_BG1 |
| 114 | MB_ACT# |
| 115 | MB_BG0 |
| 116 | DDR1_B_ALERT# |
| 117 | +V1.2DDR |
| 118 | +V1.2DDR |
| 119 | MB_MA12 |
| 120 | MB_MA11 |
| 121 | MB_MA9 |
| 122 | MB_MA7 |
| 123 | +V1.2DDR |
| 124 | +V1.2DDR |
| 125 | MB_MA8 |
| 126 | MB_MA5 |
| 127 | MB_MA6 |
| 128 | MB_MA4 |
| 129 | +V1.2DDR |
| 130 | +V1.2DDR |

| | |
|---|---|
| 131 | MB_MA3 |
| 132 | MB_MA2 |
| 133 | MB_MA1 |
| 134 | DDR1_B_EVENT# |
| 135 | +V1.2DDR |
| 136 | +V1.2DDR |
| 137 | MB_CLK_DDRB0+ |
| 138 | MB_CLK_DDRB1+ |
| 139 | MB_CLK_DDRB0- |
| 140 | MB_CLK_DDRB1- |
| 141 | +V1.2DDR |
| 142 | +V1.2DDR |
| 143 | DDR1_B_PARITY |
| 144 | MB_MA0 |
| 145 | MB_BA1 |
| 146 | MB_MA10 |
| 147 | +V1.2DDR |
| 148 | +V1.2DDR |
| 149 | MB_SCS#0 |
| 150 | MB_BA0 |
| 151 | MB_SWE# |
| 152 | MB_SRAS# |
| 153 | +V1.2DDR |
| 154 | +V1.2DDR |
| 155 | MB_ODT0 |
| 156 | MB_SCAS# |
| 157 | MB_SCS#1 |
| 158 | MB_MA13 |
| 159 | +V1.2DDR |
| 160 | +V1.2DDR |
| 161 | MB_ODT1 |
| 162 | |
| 163 | +V1.2DDR |
| 164 | DDR1_VREF_Z_DQ |
| 165 | |
| 166 | DIMMB_SA2 |
| 167 | GND |
| 168 | GND |
| 169 | MB_MD38 |
| 170 | MB_MD34 |
| 171 | GND |
| 172 | GND |
| 173 | MB_MD35 |
| 174 | MB_MD39 |
| 175 | GND |
| 176 | GND |
| 177 | MB_DQS4- |
| 178 | +V1.2DDR |

| | |
|---|---|
| 179 | MB_DQS4+ |
| 180 | GND |
| 181 | GND |
| 182 | MB_MD36 |
| 183 | MB_MD33 |
| 184 | GND |
| 185 | GND |
| 186 | MB_MD37 |
| 187 | MB_MD32 |
| 188 | GND |
| 189 | GND |
| 190 | MB_MD44 |
| 191 | MB_MD40 |
| 192 | GND |
| 193 | GND |
| 194 | MB_MD45 |
| 195 | MB_MD41 |
| 196 | GND |
| 197 | GND |
| 198 | MB_DQS5- |
| 199 | +V1.2DDR |
| 200 | MB_DQS5+ |
| 201 | GND |
| 202 | GND |
| 203 | MB_MD42 |
| 204 | MB_MD47 |
| 205 | GND |
| 206 | GND |
| 207 | MB_MD46 |
| 208 | MB_MD43 |
| 209 | GND |
| 210 | GND |
| 211 | MB_MD52 |
| 212 | MB_MD49 |
| 213 | GND |
| 214 | GND |
| 215 | MB_MD48 |
| 216 | MB_MD53 |
| 217 | GND |
| 218 | GND |
| 219 | MB_DQS6- |
| 220 | +V1.2DDR |
| 221 | MB_DQS6+ |
| 222 | GND |
| 223 | GND |
| 224 | MB_MD55 |
| 225 | MB_MD50 |
| 226 | GND |

| | |
|---|---|
| 227 | GND |
| 228 | MB_MD54 |
| 229 | MB_MD51 |
| 230 | GND |
| 231 | GND |
| 232 | MB_MD60 |
| 233 | MB_MD57 |
| 234 | GND |
| 235 | GND |
| 236 | MB_MD56 |
| 237 | MB_MD61 |
| 238 | GND |
| 239 | GND |
| 240 | MB_DQS7- |
| 241 | +V1.2DDR |
| 242 | MB_DQS7+ |
| 243 | GND |
| 244 | GND |
| 245 | MB_MD62 |
| 246 | MB_MD63 |
| 247 | GND |
| 248 | GND |
| 249 | MB_MD59 |
| 250 | MB_MD58 |
| 251 | GND |
| 252 | GND |
| 253 | SMB_CLK |
| 254 | SMB_DAT |
| 255 | +V3.3 |
| 256 | DIMMB_SAO |
| 257 | +V2.5_VPP |
| 258 | +V0.6  VTT |
| 259 | +V2.5_VPP |
| 260 | DIMMB_SA1 |
| H1 | NC |
| H2 | NC |
| H3 | GND |
| H4 | GND |

## A.3.13 DDR4 SODIMM 260P/H9.2mm




| Pin | Signal Pin Definition |
|---|---|
| 1 | GND |
| 2 | GND |
| 3 | MA_MD4 |
| 4 | MA_MD1 |
| 5 | GND |
| 6 | GND |
| 7 | MA_MDO |
| 8 | MA_MD5 |
| 9 | GND |
| 10 | GND |
| 11 | MA_DQSO- |
| 12 | +V1.2DDR |
| 13 | MA_DQSO+ |
| 14 | GND |
| 15 | GND |
| 16 | MA_MD6 |
| 17 | MA_MD7 |
| 18 | GND |
| 19 | GND |
| 20 | MA_MD2 |
| 21 | MA_MD3 |
| 22 | GND |
| 23 | GND |
| 24 | MA_MD9 |
| 25 | MA_MD13 |
| 26 | GND |
| 27 | GND |
| 28 | MA_MD8 |
| 29 | MA_MD12 |
| 30 | GND |
| 31 | GND |
| 32 | MA_DQS1- |
| 33 | +V1.2DDR |

| | |
|---|---|
| 34 | MA_DQS1+ |
| 35 | GND |
| 36 | GND |
| 37 | MA_MD15 |
| 38 | MA_MD10 |
| 39 | GND |
| 40 | GND |
| 41 | MA_MD14 |
| 42 | MA_MD11 |
| 43 | GND |
| 44 | GND |
| 45 | MA_MD21 |
| 46 | MA_MD16 |
| 47 | GND |
| 48 | GND |
| 49 | MA_MD20 |
| 50 | MA_MD17 |
| 51 | GND |
| 52 | GND |
| 53 | MA_DQS2- |
| 54 | +V1.2DDR |
| 55 | MA_DQS2+ |
| 56 | GND |
| 57 | GND |
| 58 | MA_MD19 |
| 59 | MA_MD22 |
| 60 | GND |
| 61 | GND |
| 62 | MA_MD23 |
| 63 | MA_MD18 |
| 64 | GND |
| 65 | GND |
| 66 | MA_MD24 |
| 67 | MA_MD29 |
| 68 | GND |
| 69 | GND |
| 70 | MA_MD25 |
| 71 | MA_MD28 |
| 72 | GND |
| 73 | GND |
| 74 | MA_DQS3- |
| 75 | +V1.2DDR |
| 76 | MA_DQS3+ |
| 77 | GND |
| 78 | GND |
| 79 | MA_MD27 |
| 80 | MA_MD26 |
| 81 | GND |

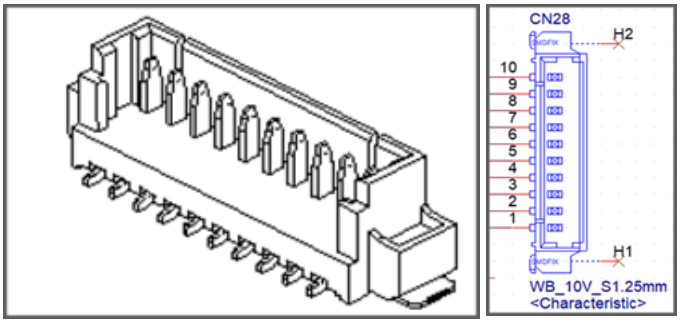
| | |
|---|---|
| 82 | GND |
| 83 | MA_MD30 |
| 84 | MA_MD31 |
| 85 | GND |
| 86 | GND |
| 87 | MA_CB5 |
| 88 | MA_CB4 |
| 89 | GND |
| 90 | GND |
| 91 | MA_CB1 |
| 92 | MA_CB0 |
| 93 | GND |
| 94 | GND |
| 95 | MA_DQS8- |
| 96 | +V1.2DDR |
| 97 | MA_DQS8+ |
| 98 | GND |
| 99 | GND |
| 100 | MA_CB6 |
| 101 | MA_CB2 |
| 102 | GND |
| 103 | GND |
| 104 | MA_CB7 |
| 105 | MA_CB3 |
| 106 | GND |
| 107 | GND |
| 108 | DDR4_DRAMRST# |
| 109 | MA_CKE0 |
| 110 | MA_CKE1 |
| 111 | +V1.2DDR |
| 112 | +V1.2DDR |
| 113 | MA_BG1 |
| 114 | MA_ACT# |
| 115 | MA_BG0 |
| 116 | DDR0_A_ALERT# |
| 117 | +V1.2DDR |
| 118 | +V1.2DDR |
| 119 | MA_MA12 |
| 120 | MA_MA11 |
| 121 | MA_MA9 |
| 122 | MA_MA7 |
| 123 | +V1.2DDR |
| 124 | +V1.2DDR |
| 125 | MA_MA8 |
| 126 | MA_MA5 |
| 127 | MA_MA6 |
| 128 | MA_MA4 |
| 129 | +V1.2DDR |

| | |
|---|---|
| 130 | +V1.2DDR |
| 131 | MA_MA3 |
| 132 | MA_MA2 |
| 133 | MA_MA1 |
| 134 | DDR0_A_EVENT# |
| 135 | +V1.2DDR |
| 136 | +V1.2DDR |
| 137 | MA_CLK_DDRA0+ |
| 138 | MA_CLK_DDRA1+ |
| 139 | MA_CLK_DDRA0- |
| 140 | MA_CLK_DDRA1- |
| 141 | +V1.2DDR |
| 142 | +V1.2DDR |
| 143 | DDR0_A_PARITY |
| 144 | MA_MA0 |
| 145 | MA_BA1 |
| 146 | MA_MA10 |
| 147 | +V1.2DDR |
| 148 | +V1.2DDR |
| 149 | MA_SCS#0 |
| 150 | MA_BA0 |
| 151 | MA_SWE# |
| 152 | MA_SRAS# |
| 153 | +V1.2DDR |
| 154 | +V1.2DDR |
| 155 | MA_ODT0 |
| 156 | MA_SCAS# |
| 157 | MA_SCS#1 |
| 158 | MA_MA13 |
| 159 | +V1.2DDR |
| 160 | +V1.2DDR |
| 161 | MA_ODT1 |
| 162 | |
| 163 | +V1.2DDR |
| 164 | DDR0_VREF_Z_CA |
| 165 | |
| 166 | DIMMA_SA2 |
| 167 | GND |
| 168 | GND |
| 169 | MA_MD33 |
| 170 | MA_MD36 |
| 171 | GND |
| 172 | GND |
| 173 | MA_MD37 |
| 174 | MA_MD32 |
| 175 | GND |
| 176 | GND |
| 177 | MA_DQS4- |

| | |
|---|---|
| 178 | +V1.2DDR |
| 179 | MA_DQS4+ |
| 180 | GND |
| 181 | GND |
| 182 | MA_MD35 |
| 183 | MA_MD38 |
| 184 | GND |
| 185 | GND |
| 186 | MA_MD34 |
| 187 | MA_MD39 |
| 188 | GND |
| 189 | GND |
| 190 | MA_MD40 |
| 191 | MA_MD44 |
| 192 | GND |
| 193 | GND |
| 194 | MA_MD45 |
| 195 | MA_MD41 |
| 196 | GND |
| 197 | GND |
| 198 | MA_DQS5- |
| 199 | +V1.2DDR |
| 200 | MA_DQS5+ |
| 201 | GND |
| 202 | GND |
| 203 | MA_MD43 |
| 204 | MA_MD47 |
| 205 | GND |
| 206 | GND |
| 207 | MA_MD46 |
| 208 | MA_MD42 |
| 209 | GND |
| 210 | GND |
| 211 | MA_MD50 |
| 212 | MA_MD48 |
| 213 | GND |
| 214 | GND |
| 215 | MA_MD52 |
| 216 | MA_MD49 |
| 217 | GND |
| 218 | GND |
| 219 | MA_DQS6- |
| 220 | +V1.2DDR |
| 221 | MA_DQS6+ |
| 222 | GND |
| 223 | GND |
| 224 | MA_MD53 |
| 225 | MA_MD54 |

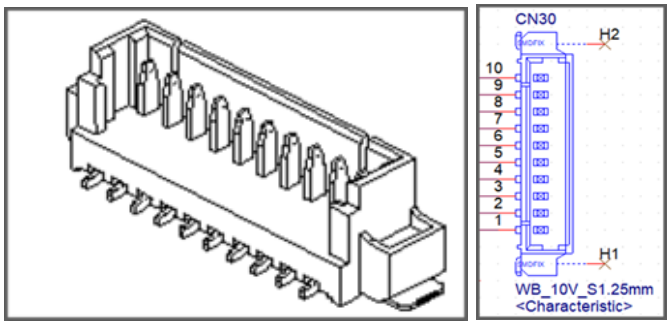
| | |
|---|---|
| 226 | GND |
| 227 | GND |
| 228 | MA_MD55 |
| 229 | MA_MD51 |
| 230 | GND |
| 231 | GND |
| 232 | MA_MD56 |
| 233 | MA_MD57 |
| 234 | GND |
| 235 | GND |
| 236 | MA_MD60 |
| 237 | MA_MD61 |
| 238 | GND |
| 239 | GND |
| 240 | MA_DQS7- |
| 241 | +V1.2DDR |
| 242 | MA_DQS7+ |
| 243 | GND |
| 244 | GND |
| 245 | MA MD62 |
| 246 | MA MD59 |
| 247 | GND |
| 248 | GND |
| 249 | MA MD58 |
| 250 | MA MD63 |
| 251 | GND |
| 252 | GND |
| 253 | SMB_CLK |
| 254 | SMB  OAT |
| 255 | +V3.3 |
| 256 | DIMMA_SAO |
| 257 | +V2.5_VPP |
| 258 | +V0.6  VTT |
| 259 | +V2.5  VPP |
| 260 | DIMMA_SA1 |
| H1 | NC |
| H2 | NC |
| H3 | GND |
| H4 | GND |

## A.3.14 GPIO/RS232 Connector



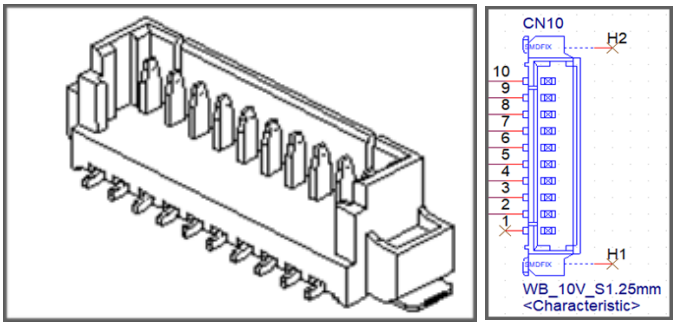

| Pin | Signal Pin Definition |
|---|---|
| 1 | GND |
| 2 | GPIO7/COM_RI# |
| 3 | GPIO2/COM_DTR# |
| 4 | GPIO6/COM_CTS# |
| 5 | GPIO1/COM_TXD |
| 6 | GPIO5/COM_RTS# |
| 7 | GPIO0/COM_RXD |
| 8 | GPIO4/COM_DSR# |
| 9 | +V5_GPIO/COM_DCD# |
| 10 | GPIO3/COM_GND |

## A.3.15 GPIO/RS232 Connector



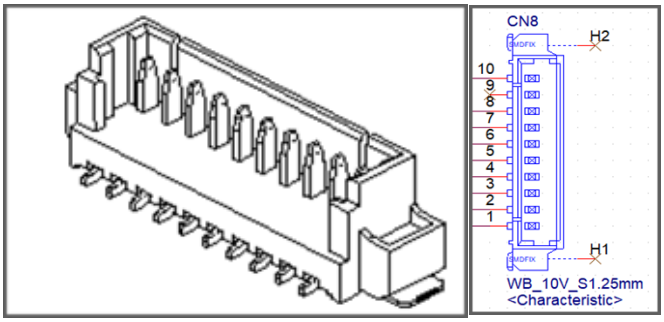

| Pin | Signal Pin Definition |
|---|---|
| 1 | GND |
| 2 | GPIO7/COM_RI# |
| 3 | GPIO2_COM_DTR# |
| 4 | GPIO6/COM_CTS# |
| 5 | GPIO1/COM_TXD |
| 6 | GPIO5/COM_RTS# |
| 7 | GPIO0/COM_RXD |
| 8 | GPIO4/COM_DSR# |
| 9 | +V5_GPIO/COM_DCD# |
| 10 | GPIO3/COM_GND |

## A.3.16 COM Port Connector (RS232+RS422+RS485)



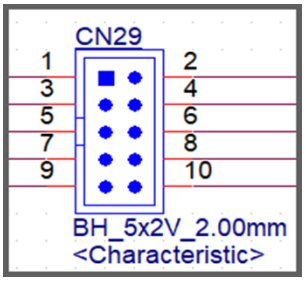

| Pin | Signal Pin Definition |
|---|---|
| 1 | NC |
| 2 | RI# |
| 3 | 422RX-/DTR# |
| 4 | CTS# |
| 5 | 422RX+/TXD |
| 6 | RTS# |
| 7 | 422TX+/485D+/RXD |
| 8 | DSR# |
| 9 | 422TX-/485D-/DCD# |
| 10 | GND |

## A.3.17 Power/LED/Case Open/Buzzer Connector



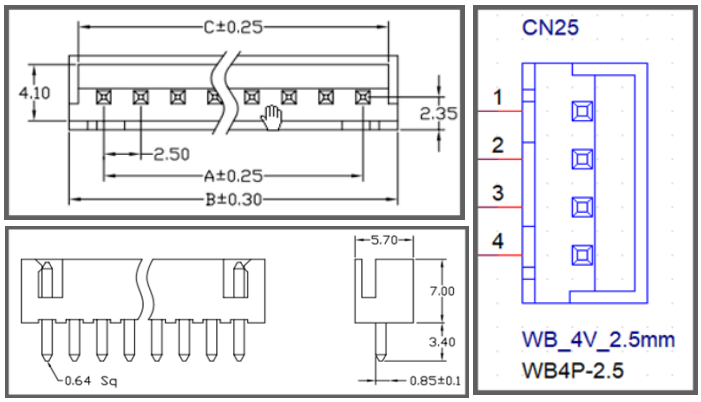

| Pin | Signal Pin Definition |
|---|---|
| 1 | GND |
| 2 | BUZZER- |
| 3 | BUZZER+ |
| 4 | CASEOPEN |
| 5 | SATA_LED# |
| 6 | PSIN# |
| 7 | RST# |
| 8 | +3.3V |
| 9 | NC |
| 10 | +5V |

## A.3.18 Audio Connector



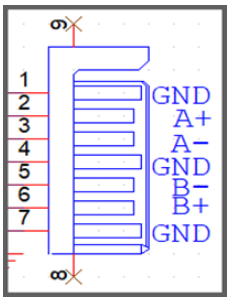

| Pin | Signal Pin Definition |
|---|---|
| 1 | LOUTR |
| 2 | LINR |
| 3 | GND |
| 4 | GND |
| 5 | LOUTL |
| 6 | LINL |
| 7 | GND |
| 8 | GND |
| 9 | MIC1R |
| 10 | MIC1L |

## A.3.19 HDD Power Connector



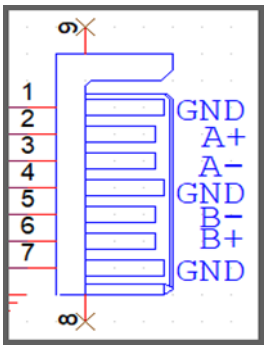

| Pin | Signal Pin Definition |
|---|---|
| 1 | 5V |
| 2 | GND |
| 3 | GND |
| 4 | 12V |

## A.3.20 HDD Connector



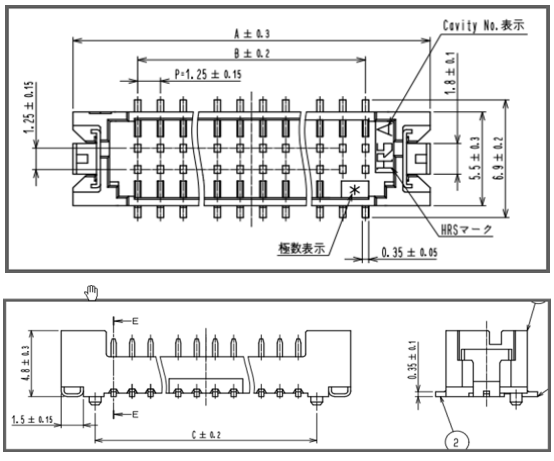

| Pin | Signal Pin Definition |
|---|---|
| 1 | GND |
| 2 | SATA0_TX+ |
| 3 | SATA0_TX- |
| 4 | GND |
| 5 | SATA0_RX- |
| 6 | SATA0_RX+ |
| 7 | GND |

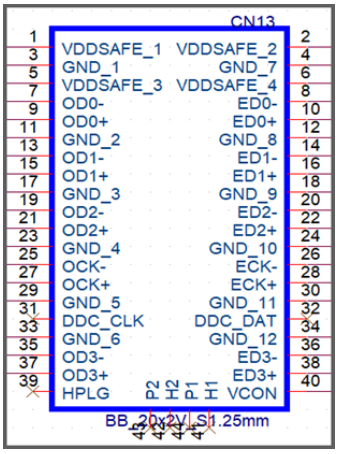
## A.3.21 HDD Connector




| Pin | Signal Pin Definition |
|---|---|
| 1 | GND |
| 2 | SATA1_TX+ |
| 3 | SATA1_TX- |
| 4 | GND |
| 5 | SATA1_RX- |
| 6 | SATA1_RX+ |
| 7 | GND |

## A.3.22 LVDS Connector

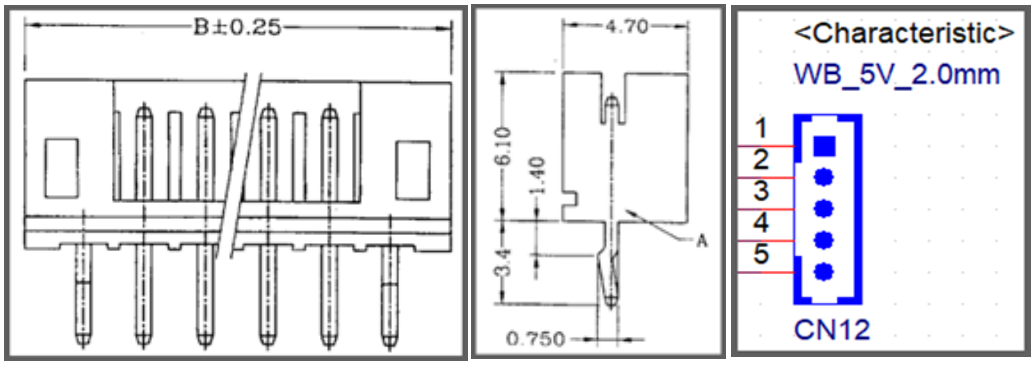



| Pin | Signal Pin Definition |
|---|---|
| 1 | +V_LCD |
| 2 | +V_LCD |
| 3 | GND |
| 4 | GND |
| 5 | +V_LCD |
| 6 | +V_LCD |
| 7 | LVDS1_0_D0- |
| 8 | LVDS1_1_D0- |
| 9 | LVDS1_0_D0+ |
| 10 | LVDS1_1_D0+ |

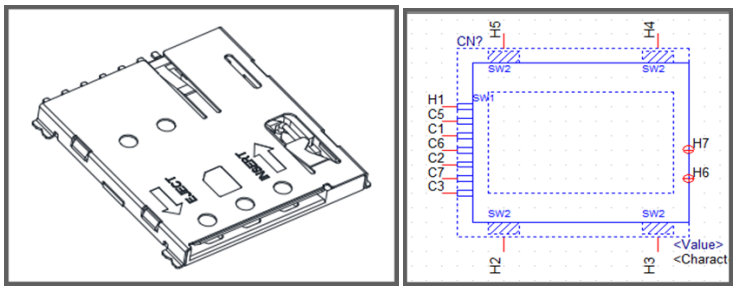
| | |
|---|---|
| 11 | GND |
| 12 | GND |
| 13 | LVDS1_0_D1- |
| 14 | LVDS1_1_D1- |
| 15 | LVDS1_0_D1+ |
| 16 | LVDS1_1_D1+ |
| 17 | GND |
| 18 | GND |
| 19 | LVDS1_0_D2- |
| 20 | LVDS1_1_D2- |
| 21 | LVDS1_0_D2+ |
| 22 | LVDS1_1_D2+ |
| 23 | GND |
| 24 | GND |
| 25 | LVDS1_0_CLK- |
| 26 | LVDS1_1_CLK- |
| 27 | LVDS1_0_CLK+ |
| 28 | LVDS1_1_CLK+ |
| 29 | GND |
| 30 | GND |
| 31 | NC |
| 32 | NC |
| 33 | GND |
| 34 | GND |
| 35 | LVDS1_0_D3- |
| 36 | LVDS1_1_D3- |
| 37 | LVDS1_0_D3+ |
| 38 | LVDS1_1_D3+ |
| 39 | NC |
| 40 | LVDS1_VCON |

## A.3.23 Panel Inverter Connector



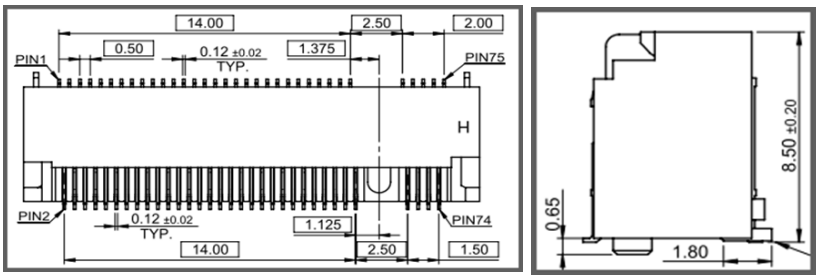

| Pin | Signal Pin Definition |
|---|---|
| 1 | +V12 |
| 2 | GND |
| 3 | LVDS1_ENABKL |
| 4 | LVDS1_PWM |
| 5 | +V5 |

## A.3.24 SIM Card Connector




| Pin | Signal Pin Definition |
|---|---|
| C1 | +VUIM_PWR |
| C2 | UIM RESET |
| C3 | UIM_CLK |
| C5 | GND |
| C6 | +VUIM_VPP |
| C7 | UIM DATA |
| H1 | SIM_DET |
| H2 | GND |
| H3 | GND |
| H4 | GND |
| H5 | GND |
| H6 | NC |
| H7 | NC |

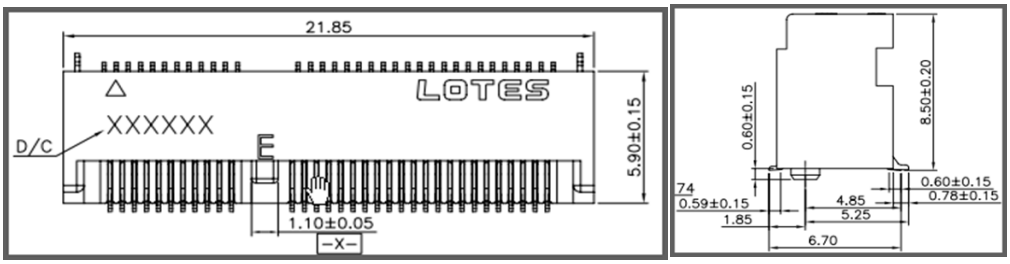
## A.3.25 Key M and Key B Connector

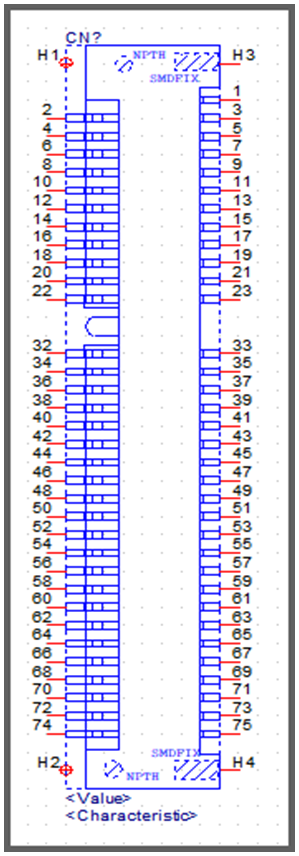



| Pin | Signal Pin Definition (Key M) | Pin | Signal Pin Definition (Key B) |
|---|---|---|---|
| 1 | M.2_CONFIG_3 (GND) | 1 | M.2_CONFIG_3 |
| 2 | +V3.3_M.2 | 2 | +V3.3_M.2 |
| 3 | GND | 3 | GND |
| 4 | +V3.3_M.2 | 4 | +V3.3_M.2 |
| 5 | PCIE_KEY-M_R_RX9- | 5 | GND |
| 6 | NC | 6 | NC |
| 7 | PCIE_KEY-M_R_RX9+ | 7 | USB7_P+ |
| 8 | WWAN_DISABLE# | 8 | WWAN_DISABLE# |
| 9 | GND | 9 | USB7_KEYB_P- |
| 10 | NC | 10 | NC |
| 11 | PCIE_A_PCH_TXN3 | 11 | GND |
| 12 | +V3.3_M.2 | 12 | B Key NC |
| 13 | PCIE_A_PCH_TXP3 | 13 | |
| 14 | +V3.3_M.2 | 14 | |
| 15 | GND | 15 | |
| 16 | +V3.3_M.2 | 16 | |
| 17 | PCIE_KEY-M_RX8- | 17 | |
| 18 | +V3.3_M.2 | 18 | |
| 19 | PCIE_KEY-M_RX8+ | 19 | |
| 20 | NC | 20 | NC |
| 21 | M.2_CONFIG_0 (GND) | 21 | M.2_CONFIG_0 |
| 22 | NC | 22 | NC |
| 23 | PCIE_A_PCH_TXN2 | 23 | PCIE_A_PCH_TXN2 |
| 24 | NC | 24 | NC |
| 25 | PCIE_A_PCH_TXP2 | 25 | PCIE_A_PCH_TXP2 |
| 26 | NC | 26 | NC |
| 27 | GND | 27 | GND |
| 28 | NC | 28 | NC |
| 29 | PCIE_KEY-M_RX7- | 29 | PCIE_KEY-M_RX7- |
| 30 | UIM_A_RESET | 30 | UIM_A_RESET |
| 31 | PCIE_KEY-M_RX7+ | 31 | PCIE_KEY-M_RX7+ |
| 32 | UIM_A_CLK | 32 | UIM_A_CLK |
| 33 | GND | 33 | GND |
| 34 | UIM_A_DATA | 34 | UIM_A_DATA |
| 35 | PCIE_A_PCH_TXN1 | 35 | PCIE_A_PCH_TXN1 |
| 36 | +VUIM_A_PWR | 36 | +VUIM_A_PWR |

| | | | |
|---|---|---|---|
| 37 | PCIE_A_PCH_TXP1 | 37 | PCIE_A_PCH_TXP1 |
| 38 | NC | 38 | NC |
| 39 | GND | 39 | GND |
| 40 | NC | 40 | NC |
| 41 | MPCIE_MSATA_RX+ | 41 | MPCIE_MSATA_RX+ |
| 42 | NC | 42 | NC |
| 43 | MPCIE_MSATA_RX- | 43 | MPCIE_MSATA_RX- |
| 44 | NC | 44 | NC |
| 45 | GND | 45 | GND |
| 46 | NC | 46 | NC |
| 47 | MPCIE_MSATA_TX- | 47 | MPCIE_MSATA_TX- |
| 48 | NC | 48 | NC |
| 49 | MPCIE_MSATA_TX+ | 49 | MPCIE_MSATA_TX+ |
| 50 | PLTRST_MKEY_BUFFER# | 50 | NC |
| 51 | GND | 51 | GND |
| 52 | CLK2_M2MB_A_PCIE_REQ# | 52 | CLK2_M2MB_A_PCIE_REQ# |
| 53 | CK_100M_A_MKEY_N | 53 | CK_100M_A_MKEY_N |
| 54 | M.2_PCIE_WAKE# | 54 | M.2_PCIE_WAKE# |
| 55 | CK_100M_A_MKEY_P | 55 | CK_100M_A_MKEY_P |
| 56 | NC | 56 | NC |
| 57 | GND | 57 | GND |
| 58 | NC | 58 | NC |
| 59 | M Key NC | 59 | NC |
| 60 | | 60 | NC |
| 61 | | 61 | NC |
| 62 | | 62 | NC |
| 63 | | 63 | NC |
| 64 | | 64 | NC |
| 65 | | 65 | NC |
| 66 | | 66 | SIM_KEYB_DET |
| 67 | M.2_RESET#_R | 67 | M.2_RESET#_R |
| 68 | PCH_SUSCLK_R_MKEY | 68 | PCH_SUSCLK_R_MKEY |
| 69 | M2_SSD_PEDET | 69 | M2_SSD_PEDET |
| 70 | +V3.3_M.2 | 70 | +V3.3_M.2 |
| 71 | GND | 71 | GND |
| 72 | +V3.3_M.2 | 72 | +V3.3_M.2 |
| 73 | GND | 73 | GND |
| 74 | +V3.3_M.2 | 74 | +V3.3_M.2 |
| 75 | GND | 75 | GND |

## A.3.26 Key E Connector



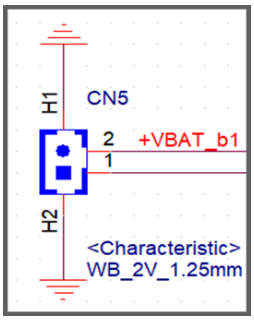




| Pin | Signal Pin Definition (Key E) |
|---|---|
| 1 | GND |
| 2 | +V3.3SB_M.2_E |
| 3 | USB6 Z P+ |
| 4 | +V3.3SB_M.2_E |
| 5 | USB6_Z_P- |
| 6 | NC |
| 7 | GND |
| 8 | NC |
| 9 | NC |
| 10 | NC |
| 11 | NC |
| 12 | NC |
| 13 | NC |
| 14 | NC |

| | |
|---|---|
| 15 | NC |
| 16 | NC |
| 17 | NC |
| 18 | GND |
| 19 | NC |
| 20 | NC |
| 21 | NC |
| 22 | NC |
| 23 | |
| 24 | |
| 25 | |
| 26 | |
| 27 | E Key NC |
| 28 | |
| 29 | |
| 30 | |
| 31 | |
| 32 | NC |
| 33 | GND |
| 34 | NC |
| 35 | PCIE_M2_Z_TX7+ |
| 36 | NC |
| 37 | PCIE_M2_Z_TX7- |
| 38 | NC |
| 39 | GND |
| 40 | NC |
| 41 | PCIE_M2_RX7+ |
| 42 | NC |
| 43 | PCIE_M2_RX7- |
| 44 | NC |
| 45 | GND |
| 46 | NC |
| 47 | CLK_M2E_Z_PCIE+ |
| 48 | NC |
| 49 | CLK_M2E_Z_PCIE- |
| 50 | SUSCLK_Z_EKEY |
| 51 | GND |
| 52 | PLTRST_BUFFER# |
| 53 | PCIE_A_CLKREQ2# |
| 54 | BT_DISABLE# |
| 55 | PCIE_WAKE# |
| 56 | WIFI_DISABLE# |
| 57 | GND |
| 58 | I2C0_KEYE_DAT |
| 59 | NC |
| 60 | I2C0_KEYE_CLK |
| 61 | NC |
| 62 | NC |

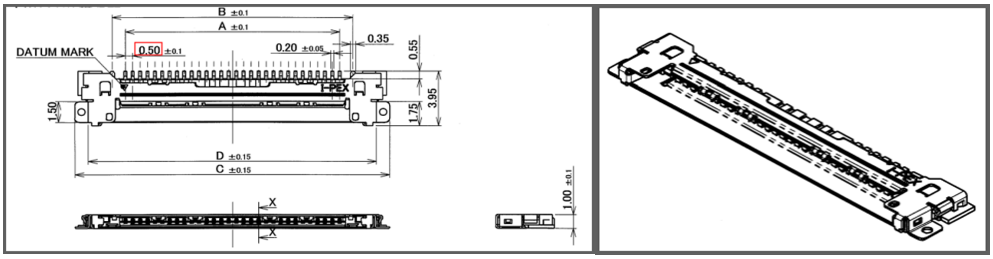
| | |
|---|---|
| 63 | GND |
| 64 | NC |
| 65 | NC |
| 66 | NC |
| 67 | NC |
| 68 | NC |
| 69 | GND |
| 70 | NC |
| 71 | NC |
| 72 | +V3.3SB_M.2_E |
| 73 | NC |
| 74 | +V3.3SB_M.2_E |
| 75 | GND |

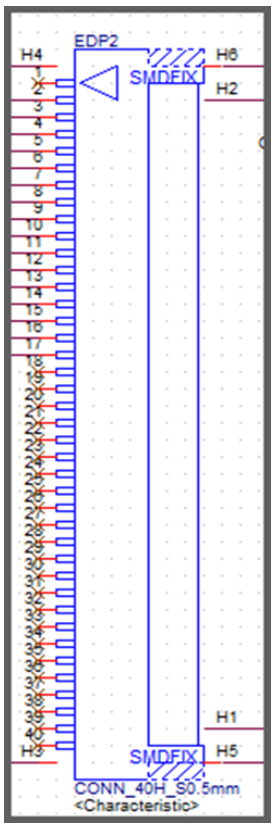
## A.3.27 RTC Battery Connector




| Pin | Signal Pin Definition (Key M) |
|---|---|
| 1 | +VBAT |
| 2 | GND |

## A.3.28 eDP Connector

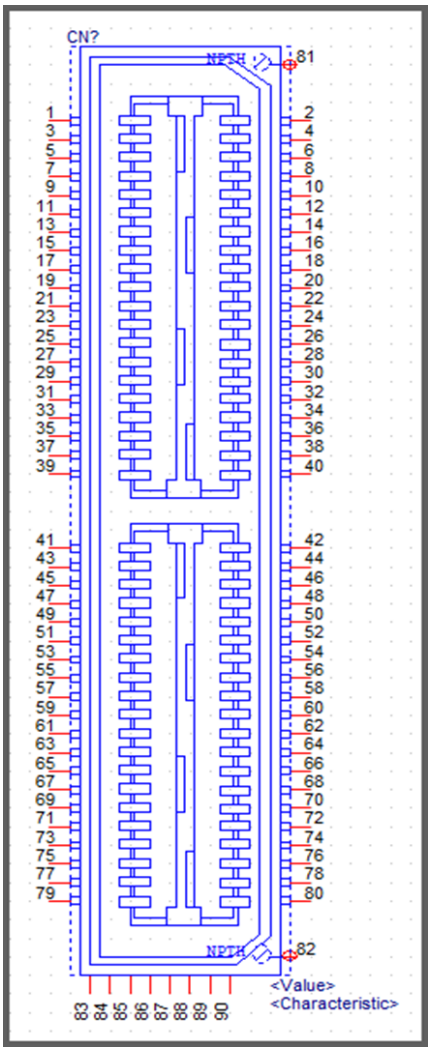





| Pin | Signal Pin Definition |
|---|---|
| 1 | NC |
| 2 | GND |
| 3 | EDP_Z_TX3- |
| 4 | EDP_Z_TX3+ |
| 5 | GND |
| 6 | EDP_Z_TX2- |
| 7 | EDP_Z_TX2+ |
| 8 | GND |
| 9 | EDP_Z_TX1- |
| 10 | EDP_Z_TX1+ |
| 11 | GND |
| 12 | EDP_Z_TXO- |
| 13 | EDP_Z_TXO+ |
| 14 | GND |
| 15 | EDP_Z_AUX+ |
| 16 | EDP_Z_AUX- |
| 17 | GND |
| 18 | +V_LCD |
| 19 | +V_LCD |
| 20 | +V_LCD |
| 21 | +V_LCD |
| 22 | NC |
| 23 | GND |
| 24 | GND |

| | |
|---|---|
| 25 | GND |
| 26 | GND |
| 27 | DDP3_EDP_Z_HPD |
| 28 | GND |
| 29 | GND |
| 30 | GND |
| 31 | GND |
| 32 | LVDS1_z_ENABKL |
| 33 | EC_LVDS1_z_PWM |
| 34 | NC |
| 35 | NC |
| 36 | +V12_+V5_EDP_INVERTER_O |
| 37 | +V12_+V5_EDP_INVERTER_O |
| 38 | +V12_+V5_EDP_INVERTER 0 |
| 39 | +V12_+V5_EDP_INVERTER_O |

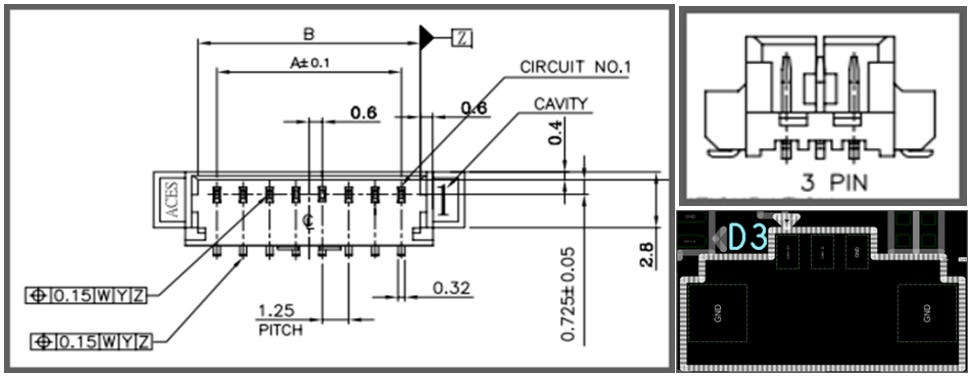
## A.3.29 MIOe Connector



| Pin | Signal Pin Definition (Key M) |
|---|---|
| 1 | GND |
| 2 | GND |
| 3 | PCIE_MIO_RX1+ |
| 4 | PCIE_MIO_A_TX1+ |
| 5 | PCIE_MIO_RX1- |
| 6 | PCIE_MIO_A_TX1- |
| 7 | GND |
| 8 | GND |
| 9 | PCIE_MIO_RX2+ |
| 10 | PCIE_MIO_A_TX2+ |
| 11 | PCIE_MIO_RX2- |
| 12 | PCIE_MIO_A_TX2- |
| 13 | GND |
| 14 | GND |
| 15 | PCIE_MIO_RX3+ |
| 16 | PCIE_MIO_A_TX3+ |
| 17 | PCIE_MIO_RX3- |
| 18 | PCIE_MIO_A_TX3- |
| 19 | GND |
| 20 | GND |
| 21 | PCIE_MIO_RX4+ |
| 22 | PCIE_MIO_A_TX4+ |
| 23 | PCIE_MIO_RX4- |
| 24 | PCIE_MIO_A_TX4- |
| 25 | GND |
| 26 | GND |
| 27 | CLK5_PCIE_MIO+ |
| 28 | LOUTL_MIO |
| 29 | CLK5_PCIE_MIO- |
| 30 | LOUTR_MIO |
| 31 | GND |
| 32 | NC |
| 33 | SMB_STB_CLK |
| 34 | NC |
| 35 | SMB_STB_DAT |
| 36 | NC |
| 37 | PCIE_WAKE# |
| 38 | NC |
| 39 | PLTRST_BUFFER# |
| 40 | NC |
| 41 | PM_SLP_S3# |
| 42 | CLKOUT_MIO |
| 43 | NC |
| 44 | LPC_AD0 |
| 45 | NC |
| 46 | LPC_AD1 |

| | |
|---|---|
| 47 | GND |
| 48 | LPC_AD2 |
| 49 | NC |
| 50 | LPC_AD3 |
| 51 | NC |
| 52 | NC |
| 53 | GND |
| 54 | LPC_SERIRQ |
| 55 | NC |
| 56 | LPC_FRAME# |
| 57 | NC |
| 58 | GND |
| 59 | GND |
| 60 | USB5_P+ |
| 61 | NC |
| 62 | USB5_P- |
| 63 | NC |
| 64 | GND |
| 65 | GND |
| 66 | NC |
| 67 | NC |
| 68 | NC |
| 69 | NC |
| 70 | GND |
| 71 | GND |
| 72 | NC |
| 73 | NC |
| 74 | NC |
| 75 | NC |
| 76 | GND |
| 77 | GND |
| 78 | USB5_OC#3 |
| 79 | +V12SB_MIO |
| 80 | +V12SB_MIO |
| 81 | NC |
| 82 | NC |
| 83 | GND |
| 84 | GND |
| 85 | GND |
| 86 | GND |
| 87 | +V5SB |
| 88 | +V5SB |
| 89 | +V5SB |
| 90 | +V5SB |

## A.3.30 CANBus Connector




| Name | Net Name |
|---|---|
| 1 | CAN1_D+ |
| 2 | CAN1_D- |
| 3 | GND |

# Appendix B

## System Assignments

- System I/O Ports
- DMA Channel Assignments
- First MB Memory Map
- Interrupt Assignments

# B.1 System I/O Ports

| Table B.1: System I/O Ports | |
|---|---|
| **Addr. Range (Hex)** | **Device** |
| 00-1F | DMA Controller |
| 20-2D | Interrupt Controller |
| 2E - 2F | Motherboard Resources |
| 4E - 4F | Motherboard Resources |
| 50-52 | Timer/Counter |
| 60-6F | 8042 (Keyboard Controller) |
| 70-7F | Real-Time Clock, Non-Maskable Interrupt (NMI) Mask |
| 80-9F | DMA Page Register |
| A0-BF | Motherboard Resources |
| C0-DF | DMA Controller |
| 299-29A | EC HM Index Port and Data Port |
| 29C-29D | EC Index Port and Data Port |
| 2F8-2FF | Communications Port (COM2) |
| 3C0-3DF | Motherboard Resources |
| 3F8-3FF | Communications Port (COM1) |
| 4D0-4D1 | Motherboard Resources |

# B.2 DMA Channel Assignments

| Table B.2: DMA Channel Assignments | |
|---|---|
| **Channel** | **Function** |
| 0 | Available |
| 1 | Available |
| 2 | Available |
| 3 | Available |
| 4 | Direct Memory Access Controller |
| 5 | Available |
| 6 | Available |
| 7 | Available |

# B.3 First MB Memory Map

| Table B.3: First MB Memory Map | |
|---|---|
| **Addr. Range (Hex)** | **Device** |
| E0000h - FFFFFh | System Board |
| D0000h - DFFFFh | PCI Bus |
| C0000h - CFFFFh | System Board |
| A0000h - BFFFFh | PCI Bus |
| A0000h - BFFFFh | Intel® HD Graphic |
| 00000h - 9FFFFh | System Board |

# B.4 Interrupt Assignments

**Table B.4: Interrupt Assignments**

| Interrupt# | Interrupt Source |
|---|---|
| NMI | Parity Error Detected |
| IRQ0 | System Timer |
| IRQ1 | Using SERIRQ, Keyboard Emulation |
| IRQ2 | Interrupt from Controller 2 (Cascade) |
| IRQ3 | Communications Port (COM2) |
| IRQ4 | Communications Port (COM1) |
| IRQ5 | EC Watch DOG |
| IRQ6 | Available |
| IRQ7 | Available |
| IRQ8 | System CMOS/Real Time Clock |
| IRQ9 | Microsoft ACPI-Compliant System |
| IRQ10 | Available |
| IRQ11 | SATA Controller |
| IRQ12 | Available |
| IRQ13 | Numeric Data Processor |
| IRQ14 | Reserved |
| IRQ15 | Reserved |

# Appendix C

## Watchdog Timer Sample Code

## C.1 Watchdog Timer Sample Code

```
EC_Command_Port = 0x29Ah
EC_Data_Port = 0x299h
Write EC HW Ram = 0x89
Watch Dog Event Flag = 0x57
Watchdog Reset Delay Time = 0x5E
Reset Event = 0x04
Start WDT Function = 0x28
Stop WDT Function = 0x29
Reset WDT Function = 0x2A
================================================
.model small
.486p
.stack 256
.data
.code
org 100h
.STARTup

mov dx, EC_Command_Port
mov al,89h          ; Write EC HW ram.
out dx,al

mov dx, EC_Data_Port
mov al, 5Eh         ; Watchdog reset delay time high byte index.
out dx,al

mov dx, EC_Data_Port
mov al, 00h         ;Set 0 seconds delay time.
out dx,al

mov dx, EC_Data_Port
mov al,5Fh          ; Watchdog reset delay time low byte index.
out dx,al

mov dx, EC_Data_Port
mov al, 30h         ; Set 3 seconds delay time.
out dx,al

mov dx, EC_Command_Port
mov al, 89h          ; Write EC HW ram.
out dx,al

mov dx, EC_Data_Port
mov al,57h          ; Watch dog event flag.
out dx,al
```

```
mov dx, EC_Data_Port
mov al, 04h             ; Reset event.
out dx,al

mov dx, EC_Command_Port
mov al,28h              ; start WDT function. (stop: 0x29, reset: 0x2A)
out dx,al

.exit
END
```

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